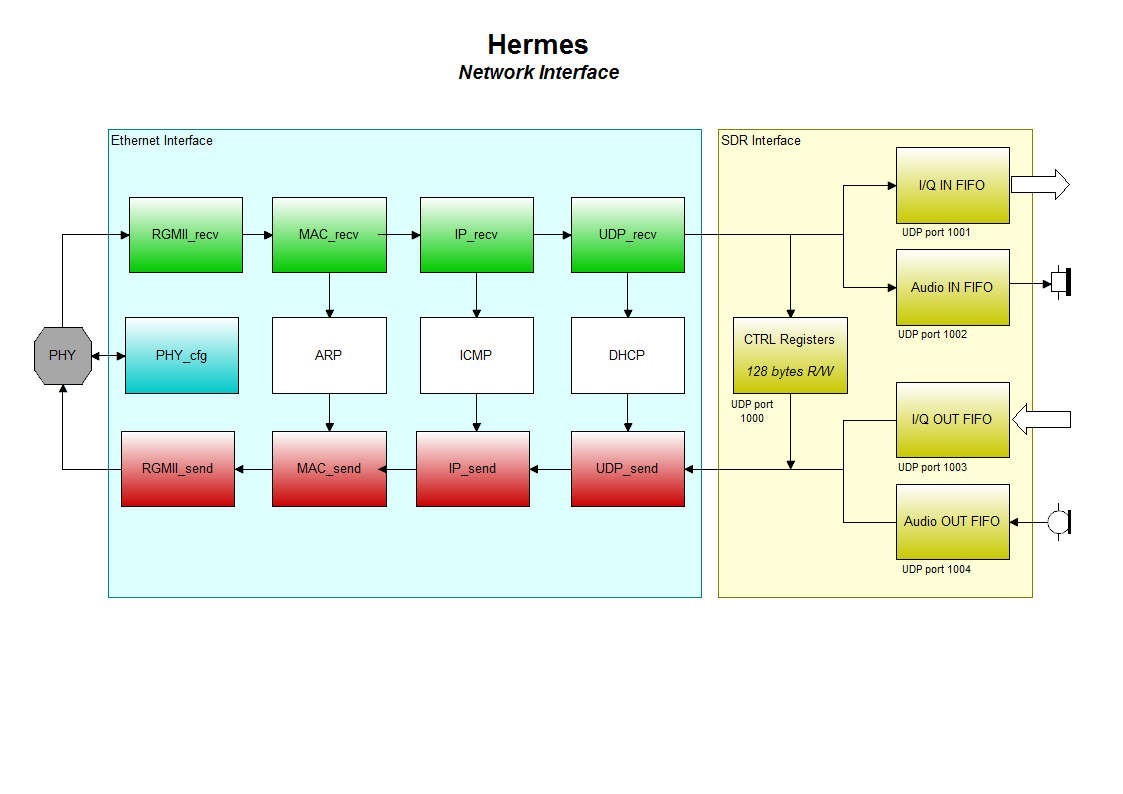
openHPSDR Ethernet Protocol

V4.0

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Revisions

|  |  |  |  |
| --- | --- | --- | --- |
| **Rev** | **Date** | **Changes** | **By** |
| 1.0 | 20 June 2015 | First release | VK6PH |
| 1.1 | 27 June 2015 | Changed Hermes Lite reference number from 5 to 6. Added DSP clock frequency and number of DDCs implemented to Discovery reply. Enable either DDC and DUC frequency or phase word to be sent to hardware. Added memory mapped registers. | VK6PH KF7O |
| 1.2 | 1 July 2015 | Added version of Protocol implemented and frequency or phase word required to Discovery reply packet. | VK6PH |
| 1.3 | 2 July 2015 | Corrected network format to be Network Byte Order, or Big-Endian. | N2ADR |
| 1.4 | 1 Aug 2015 | Added Wideband packets per frame to General Packet | VK6PH |

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| --- | --- | --- | --- |
| 1.5 | 27 Aug 2015 | Corrected General Packet source and destination ports. Corrected Microphone and Wideband data packets source port. Removed default Wideband data rate, added default samples per frame for ANAN-10E. Removed blank page 15. Changed discovery hardware identification numbers to allow ANAN-10E to be identified. Added full hardware description option for Discovery reply.  Added hardware time out should communications with host be lost. | VK6PH      G4ELI |
| 1.6 | 6 Sept 2015 | Added 10MHz reference PLL locked to High Priority packet | G4ELI |
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| 1.8 | 16 Oct 2015 | Added Discovery reply for ANAN-100E, clarified where DSP clock frequency is obtained. | VK6PH |
| 1.9 | 24 Oct 2015 | Various typographical errors corrected. Clarified number of samples per Ethernet packet for Audio and I&Q data. Added Appendix C – block diagram of Alex filters. | G4ELI, VK6PH |
| 2.0 | 28 Oct 2015 | Clarified Open Collector drive. Added NOTE1 and 2 on page 3 relating to PureSignal operation, DUC I&Q data and DUC architecture. Added number of general purpose ADCs support to Appendix A. Expanded Alex filter operation in Appendix C. Added note on Page 19 relating to synchronous and multiplexed DDC restrictions. | G4ELI, VK6PH, KC9XG |
| 2.1 | 9 Nov 2015 | Added additional Alex filter descriptions in Appendix D. Increased support for Alex filters from 4 to 8. NOTE: Open Collector register in High Priority packet has moved due to this. Added support for XLM format Discovery reply. Clarified PA enable and Envelope Tracking bits. Added note that ANAN-10E only has 31dB attenuator. Corrected number of I&Q samples in DDC packet. Corrected number of bytes in DDC packet. Added conversion constants for supply volts, exciter, Forward and Reverse power to Appendix A. | VK6PH, KC9XG,  G4ELI |
| 2.2 | 30 Nov 2015 | Removed conversion constants on page 38 since now in Appendix A.  Corrected number of DDC I&Q samples per packet in Appendix A.  Updated Alex diagrams in Appendix D.  Corrected number of DUC I&Q packets. Corrected DDC0 default port in Fig3. Added a note relating to the sequence that DDC I&Q samples are received in. | VK6PH, G4ELI,  KC9XG |
| 2.3 | 16 Dec 2015 | Set bits 26 & 27 in DUC Specific Packet to reserved. Added ability to send Discovery to hardware IP address or the broadcast address specific of the current subnet. – see page5. Added note regarding connecting to running hardware – see page 34, Byte 4.  Replaced 100E with 100B on page 34. Added description of DAC data feedback via a DDC for PureSignal use – note 1 on page 3 and Byte 17 on page 17. | VK6PH, G4ELI,  W5WC |

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| --- | --- | --- | --- |
| 2.4 | 26 Dec 2015 | Corrected Byte 1443 on page 17. Corrected length of IQ samples – page 28. | VK6PH, W5WC, G0ODC |
| 2.5 | 28 Dec 2015 | High Priority to Hardware Byte 4 bits [5] / [6] indicates I&Q FIFO empty/full – see page 38. | VK6PH, G0ODC,  G4ELI |
| 2.6 | 20 Feb 2016 | Replace ‘receiver’ with DDC, replace ‘Rxn’ with DDCn, replace  ‘transmitter’ with DUC, replace Txn with DUCn. Added note re DUC I&Q FIFO and re-sampling - Page 3. Added note re Drive level operation - Page 3. Changed DAC I&Q FIFO from empty/full to almost empty/almost full – Page 38. Added note that whilst in standby the  PTT output and Open Collector outputs will be deactivated – Page 3. | VK6PH, WU2O,  G4ELI |
| 2.7 | 20 Mar 2016 | Added hardware timer enable – General Packet, Byte 38 [0] – Page 13 and Page 3. | VK6PH |
| 2.8 | 13 Apr 2016 | Corrected Q Sample 237 on Page 45. | M6NNB |
| 2.9 | 4 Aug 2016 | Direct Fourier Conversion support added – Page 4. Added option for Little-Endian and I&Q data formats – see Page 15, Byte 39 and Page 37, Byte 22. | VK6PH, AD0ES |
| 3.0 | 17 Aug 2016 | Reduced Mic and Rx Audio packet lengths to 64 Samples to reduce latency – see Page 29 and 42. | VK6PH, NR0V |
| 3.1 | 29 Oct 2016 | Reserved Byte 40 of General Packet to SDR and Byte 23 of Discovery Reply Packet for future use. | AD0ES |
| 3.2 | 29 Dec 2016 | Corrected Open Collector data, Byte 1401, page 28. Added comment re reverse CW input, page 22. Page 23, byte 51 – line in gain explained. | G4ELI |
| 3.3 | 12 Feb 2017 | Added support for Orion MkII (ANAN-8000DLE) boards plus second Alex filter. See Page28, Page 35, byte 12 and Page 85. | W5WC |
| 3.4 | 10 Mar 2017 | Corrected BPF selections for Orion MkII (ANAN-8000DLE). Added Tx  LPF selection and block diagram of ANAN-8000DLE. See pages 89 &90. | W5WC, KC9XG |
| 3.5 | 3 Apr 2017 | Added IO2, IO4, IO5, IO6 & IO8 inputs to High Priority Status packet, see Byte 59, page 41. Added byte 1400 to the High Priority Data packet to provide Transverter support and Audio Mute for the ANAN8000DLE, page 28. | K5SO |
| 3.6 | 20 May 2017 | Replaced ANAN-8000DLE block diagram with corrected version. Page 89. | KC9XG |
| 3.7 | 14 Jul 2018 | Corrected number of audio and mic samples per packet from 720 to 64, Page 55 onwards. DUC I&Q FIFO almost full and almost empty no longer supported, see pages 4 and 41. Updated ANAN-8000DLE drawing and added ANAN-7000DLE drawing and Alex data registers. Removed Mux facility since was duplication of synchronisation feature. Added note regarding switching between synchronous modes, page 2. Added note regarding speed High Priority Status packet is sent normally and during Tx, page 40 | AD0ES, G4ELI,  KC9XG, VK6PH |
| 3.8 | 27 Mar 2019 | Corrected sidetone level, Tx Specific Packet, Byte 6 – page 23, 0 – 127. Corrected Open Collector mappings – page 29. Added ‘Beta version’ of code – Discovery Reply Packet, byte 23.  Added 16 bit check sum to programming data in order to verify correct receipt – Command Reply Packet, bytes 13 & 14. NOTE: Versions of FPGA code released after this date may include this feature. Please see individual board release notes. | VK6PH, G4ELI,  N1GP |
| 3.9 | 10 Aug 2022 | Added ethernet phy auto-negotiate 100T or 1000T and ability to force 100T. Also added reporting sequence errors from host side data. | N1GP |
| 4.0 | 13/4/2023 | Added SATURN board type | G8NJJ |

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Thanks also to Alex, VE3NEA, for the original suggestion of using UDP ports to send and receive data from.

Special thanks to Scotty, WA2DFI, for his detail analysis of the early drafts of this protocol and numerous significant contributions.

The follow have provided input and review of the protocol during its development:

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Vasiliy - K3IT, Tom - N5EG, Edson - PY2SDR, Dave - KV0S, Alex - VE3NEA, John – G0ODC, Francis - ON5RF, Alberto – I2PHD, David - WA8YWQ, Roger – W3SZ, Bob - G3UKB, Steve-K7FO, Scott – WU2O, Steve – AD0ES, Rick – N1GP.

Thanks to William, KC9XG, for preparing the Alex filter block diagrams.

Thanks also to those contributors who wish to remain anonymous.

# Purpose

This specification describes the protocol used to communicate with current and future openHPSR hardware. Its intended audience is hardware and software developers who wish to develop, or modify, hardware and software to use this architecture and protocol.

# Architecture

The basic architecture is built on the concept of using UDP ports to send and receive signals and Command & Control data.

Some configuration settings will change infrequently and can be applied to all DDCs and DUCs. These ‘General’ settings need only be sent when the SDR hardware is first turned on or when a setting changes during operation.

Settings that need to change more frequently are sent to control registers associated with DDCs or DUCs. Settings that require near real-time responses are sent as priority packets to specific UDP ports.

Where possible the protocol does not restrict the number of configurable resources. The number of fully independent DDCs, associated with a particular analogue to digital converter (ADC), can be configured using the General settings. Similarly, the number of DDCs or DUCs that may be combined synchronously is configurable.

The basic architecture for UDP data from the Host (i.e. PC, Tablet etc) is shown in Figure 1. The UDP ports here configure General Registers (where data changes infrequently after initialisation), DUC and DDC Specific Registers and High Priority Registers (where, for example, register settings change between receive and transmit.

Figure 2 illustrates the architecture for UDP data from the SDR hardware to the Host. The ports here include the Microphone data and both wide and narrow band DDC data ports.

In both diagrams some UDP ports are predetermined. Others are set by the user and/or depending on the actual number of ADCs and DACs available on the specific SDR hardware and the number of synchronous and non-synchronous DDCs and DUCs the user wishes to configure.

Figure 3 illustrates how multiple DDCs can be configured on a specific ADC. It also shows how a specific DDC can be configured to be synchronised with other DDCs configured on other ADCs.

In general, the input of a specific DDC can be fed from a selected ADC or, for PureSignal requirements, from the data being sent to a specific DAC. Each DDC can operate independently from all others i.e. its sampling rate is set independently.

Where no synchronous DDCs are selected then the output of the DDC directly feeds a FIFO and subsequently, using its designated port, the Ethernet PHY.

Where synchronous DDCs are selected then the data from these additional DDCs are sequentially passed to the FIFO associated with the base DDC. All synchronous DDCs must operate at the same sampling rate.

Synchronous DDCs are phase coherent and are used when Diversity reception and/or PureSignal processing is required.

**NOTE: A large number of wide data paths within the FPGA have to be reconfigured in order to switch to/from synchronous mode. In order for this transition to operate correctly ALL required settings (e.g. sample rates, ADC selection etc) MUST be sent in the same configuration packet (i.e. DDC Specific Packet).**

Failure to simultaneously set all configurations may result in amplitude and phase differences between the two synchronised receivers.

The maximum number of synchronous DDCs that can be selected per base DDC is equal to the number of ADCs.

The DDC follows the conventional architecture of CORDIC, CIC filters and sinc compensating FIR filter.

Figure 4 illustrates how multiple DUCs can be configured in synchronous mode. Presently, no openHPSDR SDR hardware is able to support more than one DAC. In which case data from the FIFO connect to port 1029 (default) is connected directly to the DUC and the selection of synchronous data is not supported.

The DUC is configured as a 5 stage CIC filter and CORDIC. Note that the Host I&Q data (24 bit I&Q data at 192ksps) directly feeds the CIC filter. In which case the transmitted signal will be -1dB at +/- 22kHz. For most modes this is acceptable but should wider bandwidths be required the designer may wish to include a sinc compensation filter in the Host software.

In order to overcome any potential latency issues between the Host and SDR Hardware, RF and sidetone generation for CW is done in the SDR Hardware. This includes applying a raised cosine profile to the leading and trailing edges of the CW RF and sidetone waveforms. An Iambic Keyer is also implemented and operates in Straight, simulated Bug and Iambic A or B.

Variable frequency and amplitude sidetone is also generated in the SDR Hardware.

Time stamping of DDC I & Q packets is in accordance with the VITA-49 specification for Fractional-seconds Timestamps.

For the current hardware implementation an arbitrary limit of 80 DDCs and 8 ADCs has been applied. These limits will be removed as hardware that is capable of exceeding these settings becomes available.

Compared with the previous openHPSDR Ethernet/USB protocol, numerous new features and facilities have been added. However, we should bear in mind the 'Second-system effect' - see http://en.wikipedia.org/wiki/Second-system\_effect

# Detailed operation

Consider a network made up of multiple SDRs and multiple Hosts (e.g. PCs). Each SDR on the network has a unique IP address, and listens on fixed port 1024 for Discovery packets.

The following scenario outlines how SDRs and Hosts interact within a given network segment. It is important that multiple SDRs and multiple Hosts each running multiple applications be able to interact on one segment. Note that the term “SDR” applies to a single network connection (IP address); there may be many hardware ports associated with each single IP address.

To establish communication, one network Host will broadcast a Discovery to address <255.255.255.255:1024> from its own IP address and a source port number. In this example, assume it is from <192.168.1.10:8000>.

Every device listening on port 1024 will respond to this broadcast with a response to the Hosts IP address and source port with its IP address and port number. In this example, the SDR responds to <192.168.1.10:8000> from its own fixed address of <192.168.1.30:1024>. Now a command/response channel has been established between the SDR and the Host. This channel will be used for all SDR–to-Host and Host-to-SDR communications until one or more other streams are established.

Once a channel has been established then the General Registers and DDC and DUC Specific Registers should be set up. A High Priority packet should then be send with the ‘run’ bit set in order to start data from the Hardware.

In order to recover from a network interruption, a Command & Control packet (i.e. any C&C packet) must be sent from the host to the hardware at least every second (every 100 mS is recommended). Should a C&C packet not be received, and the hardware is in the RUN state, then the hardware will switch out of the RUN state into standby.

Whilst in standby the PTT output and Open Collector outputs will be deactivated. This is to ensure the system can’t be let in a Transmit state following a network interruption.

The session can be re-started either by sending a High Priority Packet with the RUN bit set, if the same network session is still active, or a Discovery exchange followed by re-initiation of all C&C settings and thence a High Priority Packet with the RUN bit set.

The automatic hardware reset on network or PC software failure may be disabled for debugging purposes. See the General Packet for specific details.

The format of the Ethernet packets is generally consistent in that they all commence with a 32 bit sequence number. This enables the Host and Hardware to determine if packets have been lost.

In general, configuration data that is typically required by all SDR hardware is sent at the head of a packet. Settings that are specific to openHPSDR hardware are sent at the end of a packet. This leaves room in the middle of the packet for additional register settings to be included in the future without disturbing existing settings.

RF output from the DAC(s) is controlled via a Drive setting. With current openHPSDR hardware this setting controls the current available from the associated DAC and hence the RF output. The Drive setting for a particular power output will vary with frequency. However, since the exciter and PA forward power is available the PC software can calibrate the power output verses Drive setting to ensure consistency with frequency if desired.

**NOTE1:**  The protocol provides for any ADC to be used for PureSignal RF and DAC feedback. However, due to FPGA size limitations and timing requirements, for all current implementations RF feedback will be via DDC0 and DAC feedback via DDC1. DAC data may be fed back by setting ‘n’ in ADC(n) equal to the number of ADCs fitted to the hardware.

**NOTE2:** The protocol enables a variable DUC I&Q sample width and sample rate. For all current openHPSDR implementations the sample width is set to 24 bits and sampling rate fixed at 192 ksps. In current hardware the DUC I&Q FIFO is 4096 by 48 bits wide. If the hardware contains an Audio CODEC (sourcing microphone data and sinking received audio) then the rate of sending I&Q data to the FIFO may be determined by the rate at which microphone data is being received e.g. there will be a fixed relationship between the number of microphone samples received and I&Q samples sent. In which case the FIFO is unlikely to over or underrun.

However, if an Audio CODEC is not provided, or microphone and receiver audio is not sourced from the hardware (e.g. a USB headset) then the data sample rate of the mic and receiver data will most likely not match the sample rate of the hardware. In which case there is potential for the FIFO to over or underrun.

In order to prevent this situation the status of the I&Q FIFO (e.g. almost full or almost empty) is returned in the High Priority Status packet. The presence of the FIFO status is intended to enable the PC software to pace how I&Q packets are sent in order to avoid an over or underrun situation.(SEE NOTE in next paragraph).

Rather than discarding or duplicating audio and I&Q samples in order to match the required sampling rates, it is recommended that PC code developers implement a fractional re-sampler. Note that if an Audio CODEC is fitted, but microphone data is not sourced from it, then mic data packets will still be sent to the PC. In which case the PC code may use the rate that this data is received in order to determine the rate at which I&Q samples to the DUC should be sent. **NOTE:** For code released from the date of this document the status of the I&Q FIFO has been removed since PC code developers that indicated that it is not necessary.

In order to minimise DUC latency, I&Q data should be sent as soon as sufficient data is available to full a UDP packet i.e. it is not necessary, nor desirable, to wait until 4096 by 48 bit samples are available.

**Direct Fourier Conversion (DFC) support.** From V2.9 onwards the protocol supports DFC systems. These systems undertake all Digital Signal Processing in software rather than some being done in an FPGA and the balance in software. The main additions are the ability to support Little-Endian data formats and to use either the existing 3 Byte DDC I&Q data format or float or double formats. The Discovery reply packet indicates what Endian and data formats are supported. The first general packet sent in response to the discovery reply packet is used to indicate which of the available choices will be used for all further packet transfers.

**NOTE3:** This document assumes an FPGA based hardware system is being used that uses Big-Endian data format and 3 Byte DDC I&Q data and indicates where additional options are available for DFC based systems.

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# openHPSDR Host to Hardware Protocol

The Host will communicate with the Hardware using standard UDP protocol. For FPGA based hardware Byte order shall be MSB first (Network Byte Order, or Big-Endian) and all values are interpreted as unsigned integers unless otherwise noted. For DFC based software systems Big-Endian or Little-Endian Byte order may be supported in addition to float or double data formats. The Discovery response packet indicates the options available.

IP and UDP headers are as per UDP/IP standards.

Key:

|  |
| --- |
| IP Header (24 bytes) |
| UDP Header (8 bytes) |
| UDP Data (variable bytes) |

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bits  Bytes | 0-7 | 8-15 | 16-23 | 24-31 | 32- 39 | 40-47 | 48-55 | 56-63 |
| 0 | Version/IHL | Type of  Service | Total Length | | Identification | | Flags/Fragment  Offset | |
| 8 | TTL | Protocol | Header Checksum | | Source IP Address | | | |
| 16 | Destination IP Address | | | | IP Options | | | Pad |
| 24 | Source Port | | Destination Port | | UDP Length | | UDP Checksum | |
| 32...  1443 | UDP Data | | | |  | | | |

Future diagrams will only show the UDP Data with a starting byte reference of zero.

# DISCOVERY PACKET

A Discovery packet is sent from a Host in order to determine what SDRs are present on the network, and if so, how many. The format is as follows:

|  |  |  |
| --- | --- | --- |
|  | **Discovery - PC to Hardware** |  |
| **Byte** | **To Port 1024** | **Notes** |
|  |  |  |
| 0 | Seq # | [31:24] |
| 1 | Seq # | [23:16] |
| 2 | Seq # | [15:8] |
| 3 | Seq # | [7:0] |
| 4 | 0x02 | Command - Discovery |
| 5 |  | Zero |
| 6 |  | Zero |
| 7 |  | Zero |
| 8 |  | Zero |
| ….. |  |  |
| 59 |  | Zero |

*Destination Address*

This may either be sent to the IP address of a specific SDR or a **broadcast** to Ethernet address 255.255.255.255 or the specific broadcast address of the current subnet.

*Destination Port* This will be 1024.

*Sequence Number*

A 4-byte integer set to 0x00000000.

The hardware will respond with the relevant Command Reply Packet.

**NOTE:** The discovery packed will always use this format irrespective of what Endian mode is selected.

# ERASE PACKET

An Erase packet is sent from a Host in order to erase the EEPROM on the hardware prior to programming it. The format is as follows:

|  |  |  |
| --- | --- | --- |
|  | **Erase Command - PC to Hardware** |  |
| **Byte** | **To IP Address of Hardware and Port 1024** | **Notes** |
|  |  |  |
| 0 | Seq # | [31:24] |
| 1 | Seq # | [23:16] |
| 2 | Seq # | [15:8] |
| 3 | Seq # | [7:0] |
| 4 | 0x04 | Command - Erase |
| 5 | Zero |  |
| 6 | Zero |  |
| 7 | Zero |  |
| 8 | Zero |  |
| … |  |  |
| 59 | Zero |  |

*Destination Address*

This will be the Ethernet address assigned to the hardware.

*Destination Port* This will be 1024.

*Sequence Number*

A 4-byte integer set to 0x00000000.

The hardware will respond with a Command Reply Packet confirming receipt of the Erase command and a subsequent reply when the erase has completed.

NOTE: Larger EEPROMS can take up to 15 seconds to erase. The Host program should include a timer such that if a reply has not been received within this time the user should be prompted to re-try.

# PROGRAM PACKET

A Program packet is sent from a Host in order to program the EEPROM on the hardware. The format is as follows:

|  |  |  |
| --- | --- | --- |
|  | **Program Command - PC to Hardware** |  |
| **Byte** | **To IP Address of Hardware and Port 1024** | **Notes** |
|  |  |  |
| 0 | Seq # | [31:24] |
| 1 | Seq # | [23:16] |
| 2 | Seq # | [15:8] |
| 3 | Seq # | [7:0] |
| 4 | 0x05 | Command - Program |
| 5 | # of blocks [31:24] |  |
| 6 | # of blocks [23:16] |  |
| 7 | # of blocks [15:8] |  |
| 8 | # of blocks [7:0] |  |
| 9 | Program data 0 |  |
| 10 | Program data 1 |  |
| 11 | Program data 2 |  |
| 12 | Program data 3 |  |
| 13 | Program data 4 |  |
| 14 | Program data 5 |  |
| 15 | Program data 6 |  |
| …. |  |  |
| 264 | Program data 255 |  |

*Destination Address*

This will be the Ethernet address assigned to the hardware.

*Destination Port* This will be 1024.

*Sequence Number*

A 4-byte unsigned integer representing a sequence of packets from this port. The sequence starts at 0x00000000, increments for each new packet, and rolls over after exceeding 0xFFFFFFFF.

Each port decoder keeps a separate sequence count such that the hardware can determine if a decoder is missing samples in its stream. The sequence number is set to zero when initiating a Programming sequence.

*Number of Blocks*

A 4 byte integer that indicates the total number of 256 byte blocks that will be sent from the Host to the SDR hardware.

The hardware will respond with a Command Reply Packet that requests the next block of 256 bytes be sent.

NOTE: Should the Sequence Number in the Command Reply Packet not be consistent with the sent Sequence Number then the Program process should be aborted and the user given the option to restart. An affirmative response should initiate an Erase sequence followed by a Program sequence.

# SET IP ADDRESS PACKET

A Set IP Address packet is sent from a Host in order to set the IP address of the hardware. Prior to setting an IP address a Discovery Packet should be sent and the MAC address of the hardware that's IP address is to be updated recorded.

The format is as follows:

|  |  |  |
| --- | --- | --- |
|  | **Set IP Address - PC to Hardware** | |
| **Byte** | **Broadcast to Port 1024** | **Notes** |
|  |  |  |
| 0 | Seq # | [31:24] |
| 1 | Seq # | [23:16] |
| 2 | Seq # | [15:8] |
| 3 | Seq # | [7:0] |
| 4 | 0x03 | Command - Set IP Address |
| 5 | ToMAC | MSB |
| 6 | ToMAC |  |
| 7 | ToMAC |  |
| 8 | ToMAC |  |
| 9 | ToMAC |  |
| 10 | ToMAC | LSB |
| 11 | AssignIP | MSB |
| 12 | AssignIP |  |
| 13 | AssignIP |  |
| 14 | AssignIP | LSB |
| 15 | Zero |  |
| 16 | Zero |  |
| 17 | Zero |  |
| 18 | Zero |  |
| …. |  |  |
| 59 | Zero |  |

*Destination Address*

This will be Ethernet address 255.255.255.255.

*Destination Port* This will be 1024.

*Sequence Number*

A 4-byte integer set to 0x00000000.

*MAC Address*

A 6-byte value that contains the MAC address of the hardware that’s IP address requires to be set.

*IP Address*

A 4-byte value that contains the IP address that is required to be set in the hardware’s EEPROM. This may be increased in the future to enable IPv6 addressing. Setting the IP address to 0.0.0.0 will force the hardware to use DHCP addressing.

NOTE: After the IP address has been saved in EEPROM, which will take a few seconds, the successful setting of the IP address can be verified by sending a Discovery Command. The reply from the hardware will include the new IP address.

# GENERAL PACKET TO SDR

The General packet contains data that sets infrequently changed settings of the transceiver subsystems. This data is sent when the UDP data changes and, optionally, periodically.

A General Packet should be sent following a successful Discovery exchange.

The format is as follows:

|  |  |  |
| --- | --- | --- |
|  | **Control Elements - PC to Hardware** |  |
| **Byte** | **To IP Address of Hardware and Port 1024** | **Notes** |
|  |  |  |
| 0 | Seq # | [31:24] |
| 1 | Seq # | [23:16] |
| 2 | Seq # | [15:8] |
| 3 | Seq # | [7:0] |
| 4 | 0x00 | Command |
| 5 | DDC Specific port [15:8] | Default Port # 1025 |
| 6 | DDC Specific port [7:0] |  |
| 7 | DUC Specific port [15:8] | Default Port # 1026 |
| 8 | DUC Specific port [7:0] |  |
| 9 | High Priority from PC port [15:8] | Default Port # 1027 |
| 10 | High Priority from PC port [7:0] |  |
| 11 | High Priority to PC port [15:8] | Default Port # 1025 |
| 12 | High Priority to PC port [7:0] |  |
| 13 | DDC Audio port [15:8] | Default Port # 1028 |
| 14 | DDC Audio port [7:0] |  |
| 15 | DUC0 I&Q port [15:8] | Base Port (Default Port # 1029) |
| 16 | DUC0 I&Q port [7:0] |  |
| 17 | DDC0 port [15:8] | Base Port (Default Port # 1035), DDC1 = Base Port # + 1….DDC79 = Base Port # + 79 |
| 18 | DDC0 port [7:0] |  |
| 19 | Mic samples port [15:8] | Default Port # 1026 |
| 20 | Mic samples port [7:0] |  |
| 21 | Wideband ADC0 port [15:8] | Base Port (Default Port # 1027), ADC1 = Base Port # + 1….ADC7 = Base Port # + 7 |
| 22 | Wideband ADC0 port [7:0] |  |
| 23 | Wideband Enable [7:0] | WB0 = [0], WB1 = 1…..WB7 = [7] |
| 24 | Wideband Samples per packet [15:8] | Default 512 |
| 25 | Wideband Samples per packet [7:0] |  |
| 26 | Wideband sample size | Default 16 bits |
| 27 | Wideband update rate | 0 to 255mS per frame, default 20ms per frame |
| 28 | Wideband packets per frame | Default to 32 (i.e. 16k by 16 bit samples per frame) |
| 29 | Memory mapped from PC port [15:8] | Default Port # xxxx |
| 30 | Memory mapped from PC port [7:0] |  |
| 31 | Memory mapped to PC port [15:8] | Default Port # xxxx |
| 32 | Memory mapped to PC port [7:0] |  |
| 33 | Envelope PWM\_min | [15:8] Reserved for future use |
| 34 | Envelope PWM\_min | [7:0] Reserved for future use |
| 35 | Envelope PWM\_max | [15:8] Reserved for future use |
| 36 | Envelope PWM\_max | [7:0] Reserved for future use |
| 37 | Bits - [0] Time stamp, [1] VITA-49, [2] VNA mode, [3] frequency or phase word |  |
| 38 | Bit [0] set = enable hardware timer |  |
| 39 | Select Endian and DDC I&D data format | See Below |
| 40 |  | Reserved for future use (AD0ES) |
| 41… |  | Reserved for future use |
| 56 | Bits - Atlas bus configuration | [2:0] Configuration - see below |
| 57 | Bits - 10MHz ref source | [1:0] 10MHz reference source - see below |
| 58 | Bits - PA, Apollo, Mercury, clock source | [0] = PA, 1 = Apollo, [2] = Mercury Common Frequency,  [3] Clock Source - see below |
| 59 | Bits - Alex(n) enable, 1= enable, 0 = disable | [0] = Alex 0….[7] = Alex7 |

*Source Port*

This will be set to the Source Port of the Host that initiated the Discovery Packet.

*Destination Port*

This will be set to 1024.

*Sequence Number*

A 4-byte integer set to 0x00000000.

*Bytes 5 & 6*

These two bytes form a 16 bit number that specifies the port that DDC Specific commands will be sent to. If set to zero the default port 1025 will be used.

*Bytes 7 & 8*

These two bytes form a 16 bit number that specifies the port that DUC Specific commands will be sent to. If set to zero the default port 1026 will be used.

*Bytes 9 & 10*

These two bytes form a 16 bit number that specifies the port that High Priority commands will be sent to. If set to zero the default port 1027 will be used.

*Bytes 11 & 12*

These two bytes form a 16 bit number that specifies the port that High Priority commands from the hardware will be sent from. If set to zero the default port 1025 will be used.

*Bytes 13 & 14*

These two bytes form a 16 bit number that specifies the port that DDC Audio will be sent to. If set to zero the default port 1028 will be used.

*Bytes 15 & 16*

These two bytes form a 16 bit number that specifies the port that DUC I&Q data will be sent to. If set to zero the default port 1029 will be used.

*Bytes 17 & 18*

These two bytes form a 16 bit number that specifies the port that DDC 0 I&Q data will originate from. If set to zero the default port 1035 will be used. Each subsequent DDC will increment the port number respectively e.g. DDC 1 will originate from Port + 1, DDC 2 from Port +2…..DDC 79 from Port + 79

*Bytes 19 & 20*

These two bytes form a 16 bit number that specifies the port that microphone or line in data will originate from. If set to zero the default port 1026 will be used.

*Bytes 21& 22*

These two bytes form a 16 bit number that specifies the port that wideband data from ADC0 will originate from. If set to zero the default port 1027 will be used. Each subsequent wideband data will increment the port number respectively e.g. ADC1 1 will originate from Port + 1, ADC 2 from Port +2…..ADC7 from Port + 7

*Byte 23*

Enable wideband data. A set bit enables Wideband data from an associated ADC to be sent e.g. bit 0 enables ADC0, bit1 enables ADC1 etc.

*Bytes 24 & 25*

These two bytes form a 16 bit number that specifies the number of wideband samples to use per packet. The default is 512 by 16 bits samples. (default only at present)

*Byte 26*

Sets the size of a wideband sample in bits. If set to zero the default of 16 bits will be used. (default only at present)

*Byte 27*

Sets the update rate of the wideband data in mS.

*Byte 28*

Sets the number of packets of wideband data sent per frame. The default is 32 (i.e. for defaults will send 32 \* 512 = 16k by 16 bit samples per frame). For ANAN-10E this is fixed at 1024 by 16 bit samples per frame.

*Bytes 29 & 30*

These two bytes form a 16 bit number that specifies the port that memory mapped data from the PC will be sent to. If set to zero the default port xxxx will be used.

*Bytes 31 & 32*

These two bytes form a 16 bit number that specifies the port that memory mapped data to the PC will be sent to. If set to zero the default port xxxx will be used.

*Bytes 33 & 34*

These two bytes form a 16 bit number that specifies the minimum pulse width for the Envelope Tracking PWM.

*Bytes 35 & 36*

These two bytes form a 16 bit number that specifies the maximum pulse width for the Envelope Tracking PWM.

*Byte 37*

Bits when set activate the following functions; Bit[0] – Enable time stamping of DDC I&Q packets, Bit[1] - send data using VITA-49 format, Bit[2] – select VNA mode, Bit[3] selects if the DDC and DUC frequency data is sent as frequency ([3] = 0) (in Hz) or phase word ([3] = 1). A phase word is calculated as follows:

phase\_word[31:0] = 2^32 \* frequency(Hz)/DSP clock frequency (Hz)

DSP clock frequency is dependent on the Board type and is either specified in Appendix A or, if hardware specific, then as part of the Discovery response as specified in Appendix B.

**NOTE: Currently ALL openHPSDR FGPA code requires transmit and receive phase words.**

*Byte 38*

Bit[0] when set enables the hardware reset timer. This should normally be set but can be clear to assist with software testing.

*Byte 39*

When set to zero, Big-Endian and I&Q data in 3 Byte format is selected. If indicated in the Discovery reply that they are supported then the following options can be selected.

Bit 0 = 1 Use Big-Endian data format

Bit 1 = 1 Use Little-Endian data format

Bit 2 = 1 Use 3 Byte format for DDC I&Q data

Bit 3 = 1 Use float for DDC I&Q data

Bit 4 = 1 Use double for DDC I&Q data

Bits 5, 6, 7 Reserved for future use

This data should be sent in the first General packet following a Discovery reply. This first packet must use the above format (i.e. Big-Endian). All subsequent packets will use the Endian data format specified in this first packet. See also Discovery Reply Packet, Byte 22.

*Byte 56*

This selects the Atlas bus Mercury DDC configuration as follows:

|  |
| --- |
| Configuration (Mercury) |
| 000 - single DDC |
| 001 - two DDCs |
| 010 - three DDCs |
| 011 - four DDCs |

*Byte 57*

For Atlas based systems this selects the source of the 10MHz reference clock as follows:

|  |
| --- |
| 10MHz reference source |
| 00 = 10MHz reference from Atlas bus |
| 01 = 10MHz reference from Penelope |
| 10 = 10MHz reference from Mercury |

*Byte 58*

Bit[0] when set enables the PA. When in VNA mode or when using the Transverter output, the PA stage may be disabled.

Bit[1] when set enables the Apollo automatic ATU if fitted.

For Atlas based systems, Bit [2] when set enables Mercury Common Frequency and Bit [3] selects the Clock

Source - see below

|  |
| --- |
| Clock Source |
| 0 = 122.88MHz source from Penelope |
| 1 = 122.88MHz source from Mercury |

*Byte 59*

Each bit enables the respective Alex filter board e.g. Bit [0] set enables Alex0, Bit [1] set enables Alex 1 etc.

## DDC SPECIFIC PACKET

This sets the number of ADCs and the number of DDCs associated with each ADC. It also sets DDC parameters that change infrequently. This packet is sent following a successful Discovery command and prior to a Run command or when a parameter changes and, optionally, periodically.

The format of the packet is as follows:

|  |  |  |
| --- | --- | --- |
|  | **Control Elements - PC to Hardware** | |
| **Byte** | **DDC Specific** | **Notes** |
|  |  |  |
| 0 | Seq # | [31:24] |
| 1 | Seq # | [23:16] |
| 2 | Seq # | [15:8] |
| 3 | Seq # | [7:0] |
| 4 | Number of ADCs | Max of 8 ADCs |
| 5 | Bits - Dither ADC0…7 | [0] = ADC0, [1] = ADC1….[7] = ADC7 |
| 6 | Bits - Random ADC0..7 | [0] = ADC0, [1] = ADC1….[7] = ADC7 |
| 7 | DDC Enable DDC0….DDC7 | [0] = DDC0, [1]= DDC1……[7] = DDC7 |
| 8 | DDC Enable DDC 8…. DDC 15 |  |
| 9 | DDC Enable DDC 16…. DDC 23 |  |
| 10 | DDC Enable DDC 24…. DDC 31 |  |
| 11 | DDC Enable DDC 32…. DDC 39 |  |
| 12 | DDC Enable DDC 40…. DDC 47 |  |
| 13 | DDC Enable DDC 48…. DDC 55 |  |
| 14 | DDC Enable DDC 56…. DDC 63 |  |
| 15 | DDC Enable DDC 64…. DDC 71 |  |
| 16 | DDC Enable DDC 72…. DDC 79 | [0] = DDC 72……..[7] = DDC 79 |
| 17 | ADC DDC0 | ADC(n) or DAC data that DDC 0 is allocated to |
| 18 | Sampling Rate DDC 0 | [15:8] 48/96/192/384/768/1536 |
| 19 | Sampling Rate DDC 0 | [7:0] |
| 20 | CIC1 DDC 0 | For Future use |
| 21 | CIC2 DDC 0 | For Future use |
| 22 | Sample Size DDC0 | Default 24 bits |
| 23 | ADC DDC 1 | ADC(n) or DAC data that DDC 1 is allocated to. |
| 24 | Sampling Rate DDC 1 | [15:8] |
| 25 | Sampling Rate DDC 1 | [7:0] |
| 26 | CIC1 DDC 1 |  |
| 27 | CIC2 DDC 1 |  |
| 28 | Sample Size DDC 1 |  |
| 29 | ADC DDC 2 | ADC(n) or DAC data that DDC 2 is allocated to. |
| 30 | Sampling Rate DDC 2 | [15:8] |
| 31 | Sampling Rate DDC 2 | [7:0] |
| 32 | CIC1 DDC 2 |  |
| 33 | CIC2 DDC 2 |  |
| 34 | Sample Size DDC 2 |  |
| 35 | ADC DDC 3 | ADC(n) or DAC data that DDC 3 is allocated to. |
| 36 | Sampling Rate DDC 3 | [15:8] |
| 37 | Sampling Rate DDC 3 | [7:0] |
| 38 | CIC1 DDC 3 |  |
| 39 | CIC2 DDC 3 |  |
| 40 | Sample Size DDC 3 |  |
| 41 | ADC DDC 4 | ADC(n) or DAC data that DDC 4 is allocated to. |
| 42 | Sampling Rate DDC 4 | [15:8] |
| 43 | Sampling Rate DDC 4 | [7:0] |
| 44 | CIC1 DDC 4 |  |
| 45 | CIC2 DDC 4 |  |
| 46 | Sample Size DDC 4 |  |
| … |  |  |
| … |  |  |
| 485 | ADC DDC 78 | ADC(n) or DAC data that DDC 78 is allocated to. |
| 486 | Sampling Rate DDC 78 |  |
| 487 | Sampling Rate DDC 78 |  |
| 488 | CIC1 DDC 78 |  |
| 489 | CIC2 DDC 78 |  |
| 490 | Sample Size DDC 78 |  |
| 491 | ADC DDC 79 | ADC(n) or DAC data that DDC 78 is allocated to. |
| 492 | Sampling Rate DDC 79 |  |
| 493 | Sampling Rate DDC 79 |  |
| 494 | CIC1 DDC 79 |  |
| 495 | CIC2 DDC 79 |  |
| 496 | Sample Size DDC 79 |  |
| … |  |  |
| … |  |  |
| 1363 | Sync DDC 0 | [7:0] If bit set then DDC (n) is synched to DDC 0 |
| 1364 | Sync DDC 1 | [7:0] If bit set then DDC (n) is synched to DDC 1 |
| 1365 | Sync DDC 2 | [7:0] If bit set then DDC (n) is synched to DDC 2 |
| … |  |  |
| 1442 | Sync DDC 79 | [7:0] If bit set then DDC (n) is synched to DDC 79 |
| 1443 | Currently not used |  |

*Destination Port*

This may be set using the General packet and if zero defaults to 1025.

*Sequence Number*

A 4-byte integer set to 0x00000000.

*Byte 4*

Indicates the number of ADC that the hardware supports. This will be up to four on Atlas based systems, one on Hermes (ANAN-10/10E/100) and two on Angelia and Orion (ANAN-100D/200D),

*Byte 5*

A set bit activates Dither on the associated ADC e.g. Bit[0] actives ADC0, Bit[1] activates ADC1 etc.

*Byte 6*

A set bit activates Random on the associated ADC e.g. Bit[0] actives ADC0, Bit[1] activates ADC1 etc.

*Byte 7*

A set bit enables the associated DDC e.g. Bit[0] actives DDC 0, Bit[1] activates DDC 1 etc.

*Bytes 8 to 16*

A set bit enables DDCs 8 through 79.

*Byte 17*

Selects the ADC that DDC 0 is connected to where 0 connects to ADC0, 1 to ADC1 etc. For PureSignal use, to return the DAC data via a DDC, set the ADC selection to the number of ADCs fitted on the hardware.

*Bytes 18 and 19*

These two bytes from a 16 bit word that selects the sampling rate of DDC 0. Valid rates are 48/96/192/384/768/1536 ksps.

*Bytes 20 & 21*

For future use – to enable selection of the decimation rates of DDC 0 CIC filters.

*Byte 22*

Sets DDC 0 I&Q data sample size – default is 24 bits.

*Bytes 23 to 496*

Sets the ADC, sampling rate, CIC rates and data sample size of DDC 1 to 79 as above.

*Bytes 1363 to 1442*

Sets the DDC that DDC (n) is synchronised with. If a bit is set then DDC (n) is synchronised to the associated DDC. See the description of synchronous DDCs that follows.

*Byte 1443*

Currently not used.

*Synchronous DDCs*

NOTE: The sampling rate of all Synchronous DDCs must be the same and is the responsibility of the PC Control program to ensure this.

DDCs that are connected to a base DDC are usually disabled so they are not also sent from an Ethernet port. It is the responsibility of the PC Control program to ensure this.

The selection code will allow unsuitable or unnecessary DDC combinations e.g. DDC 0 + DDC 0 or DDC 0 + DDC 1 and DDC 1 + DDC 0. It is the responsibility of the PC Control program to prevent this.

There is no special provision for PureSignal operation. For PureSignal use, the PC Control program is responsible for setting the sampling rates, selecting DAC data as the source for one DDC and selecting either Synchronous or Multiplex operation of the RF and DAC DDC.

*Synchronous DDCs*: (where a number of DDCs are phase synchronous)

The maximum number of synchronised DDCs is equal to the number of ADCs.

For synchronous DDCs, if SyncDDC[n] is > 0 then DDC[n] is synchronised with another DDC(s). The bit(s) set indicate which DDC(s) are synchronised e.g. bit[0] = DDC0, bit[1] = DDC1........bit[7] = DDC7.

All DDC’s frequencies will be set to the frequency of the base DDC. If SyncDDC[n] is = 0 then there are no synchronous DDCs selected.

**NOTE:** For the time being, due to FPGA size limitations and timing closure issues only DDC0 and DDC1 may be synchronised with synchronised data presented from DDC0’s output.

SyncDDC[n] bits [7:0] when set indicate which DDC(s) are synchronised e.g. bit[0] = DDC0, bit[1] = DDC1........bit[7] = DDC7.

**NOTE:** For the time being, due to FPGA size limitations and timing closure issues, only DDC0 and DDC1 may be synchronised with synchronised data presented from DDC0 ‘s output.

## TRANSMITER SPECIFIC PACKET

This sets the number of DACs and DUC parameters that change infrequently. This packet is sent following a successful Discovery command and prior to a Run command or when a parameter changes and, optionally, periodically.

The format of the packet is as follows:

|  |  |  |
| --- | --- | --- |
|  | **Control Elements - PC to Hardware** |  |
| **Byte** | **DUC Specific** | **Notes** |
|  |  |  |
| 0 | Seq # | [31:24] |
| 1 | Seq # | [23:16] |
| 2 | Seq # | [15:8] |
| 3 | Seq # | [7:0] |
| 4 | Number of DACs | Max of 4 |
| 5 | Bits - Mode, CW, Reverse, Key Mode | See Below |
| 6 | Sidetone Level |  |
| 7 | Sidetone Frequency (Hz) | [15:8] |
| 8 | Sidetone Frequency (Hz) | [7:0] |
| 9 | Keyer Speed |  |
| 10 | Keyer Weight |  |
| 11 | Hang delay | [15:8] |
| 12 | Hang delay | [7:0] |
| 13 | RF Delay |  |
| 14 | DUC0 Sampling Rate | [15:8] |
| 15 | DUC0 Sampling Rate | [7:0] |
| 16 | DUC0 Bits |  |
| 17..25 |  | Reserved for future use |
| 26 | DUC0 Phase Shift (0 - 359 degrees) | [15:8] Reserved for future use |
| 27 | DUC0 Phase Shift | [7:0] Reserved for future use |
| 28..33 |  | Reserved for future use |
| ... |  |  |
| … |  |  |
| 50 | Bits - line in, mic boost, Orion mic | See Below |
| 51 | Line in gain |  |
| 52..58 |  | Reserved for future use |
| 59 | Step Attenuator ADC0 on DUC0 (0 - 31dB) | Reserved for future use |

*Destination Port*

This may be set using the General packet and if zero defaults to 1026.

*Sequence Number*

A 4-byte integer set to 0x00000000.

*Byte 4*

Indicates the number of DACs the hardware supports. Presently unused.

*Byte 5*

If no bits are set then CW is not selected, otherwise indicates the selection of CW options as follows:

|  |
| --- |
| Bits - Mode, CW, Reverse, Key Mode. 0 = off, 1 = on. |
| [0] = EER |
| [1] = CW |
| [2] = Reverse CW Keys |
| [3] = Iambic |
| [4] = Sidetone |
| [5] = Mode B (Mode A if not set) |
| [6] = Strict Character Spacing |
| [7] = Break\_in |

NOTE: Setting Reverse CW Keys does not alter the actual key closures reported.

*Byte 6*

Sets the CW sidetone level, 0 = off, 127 = max

*Bytes 7 & 8*

Sets the CW sidetone frequency in Hz

*Byte 9*

Sets the CW keyer speed, 0 to 60 WPM

*Byte 10*

Sets the CW weight, 33 to 66, nominal is 50

*Bytes 11 & 12*

Sets the CW hang delay in mS

*Byte 13*

Sets the RF delay in mS

*Bytes 14 & 15*

Sets DUC0 sampling rate. For current hardware fixed at 192ksps.

*Byte 16*

Sets number of bits in the DUC I&Q data. For current hardware fixed at 24 bits per sample.

*Bytes 17 to 49.*

Reserved for future use.

*Byte 50*

Allows the selection of Line in or Microphone and Microphone selection for an Orion board (ANAN-200D) as follows:

|  |
| --- |
| Bits - line in, mic boost, Orion mic. 0 = off, 1 = on |
| [0] = Line in |
| [1] = Mic Boost |
| [2] = 0 = Orion mic PTT enabled, 1 = Orion mic PTT disabled |
| [3] = 0 = Orion mic PTT to ring and mic/mic bias to tip, 1 = Orion mic PTT to tip and mic/mic bias to ring |
| [4] = 0 = disables Orion mic bias, 1 = enables Orion microphone bias |

*Byte 51*

Selects the Line in gain, 0 = +12dB, 31 = -34.5dB in 1.5dB steps.

## DUC SYNCHRONISATION PACKET

The DUC Synchronisation packet is used to configure synchronous DUCs.

The data is sent prior to a Run command, whenever a value changes and, optionally, periodically.

For future use.

## HIGH PRIORITY DATA PACKET

A High Priority Packet is sent to the associated SDR hardware whenever data changes and may also be sent periodically. It should be sent at a higher priority than any other packet. It should be sent after a successful Discovery process after configuration is complete. The format is as follows:

|  |  |  |
| --- | --- | --- |
|  | **Control Elements - PC to Hardware Port (Default 1027)** | |
| **Byte** | **High Priority** | **Notes** |
|  |  |  |
| 0 | Seq # | [31:24] |
| 1 | Seq # | [23:16] |
| 2 | Seq # | [15:8] |
| 3 | Seq # | [7:0] |
| 4 | Bits - run, PTT(n) | [0] = run, [1] = PTT0…[4] = PTT3 |
| 5 | CWX0 | [0] = CWX, [1] = Dot, [2] = Dash |
| 6 | CWX1 | Reserved for future use |
| 7 | CWX2 | Reserved for future use |
| 8 | CWX3 | Reserved for future use |
| 9 | Frequency/phase word DDC0 | [31:24] |
| 10 |  | [23:16] |
| 11 |  | [15:8] |
| 12 |  | [7:0] |
| 13 | Frequency/phase word DDC1 | [31:24] |
| 14 |  | [23:16] |
| 15 |  | [15:8] |
| 16 |  | [7:0] |
| 17 | Frequency/phase word DDC2 | [31:24] |
| 18 |  | [23:16] |
| 19 |  | [15:8] |
| 20 |  | [7:0] |
| … |  |  |
| … |  |  |
| 325 | Frequency/phase word DDC79 | [31:24] |
| 326 |  | [23:16] |
| 327 |  | [15:8] |
| 328 |  | [7:0] |
| 329 | Frequency/phase word DUC0 | [31:24] |
| 330 | DUC0 | [23:16] |
| 331 | DUC0 | [15:8] |
| 332 | DUC0 | [7:0] |
| 333 | Frequency/phase word DUC1 | Reserved for future use |
| 334 | DUC1 | Reserved for future use |
| 335 | DUC1 | Reserved for future use |
| 336 | DUC1 | Reserved for future use |

|  |  |  |
| --- | --- | --- |
| 337 | Frequency/phase word DUC2 | Reserved for future use |
| 338 | DUC2 | Reserved for future use |
| 339 | DUC2 | Reserved for future use |
| 340 | DUC2 | Reserved for future use |
| 341 | Frequency/phase word DUC3 | Reserved for future use |
| 342 | DUC3 | Reserved for future use |
| 343 | DUC3 | Reserved for future use |
| 344 | DUC3 | Reserved for future use |
| 345 | DUC0 Drive Level | 0-255 |
| 346 | DUC1 Drive Level | Reserved for future use |
| 347 | DUC2 Drive Level | Reserved for future use |
| 348 | DUC3 Drive Level | Reserved for future use |
| … |  |  |
| 1400 | Transverter and Audio enable | [7:0] |
| 1401 | Open Collector Outputs | [1] = Open Collector 1......[7] = Open  Collector 7 |
| 1402 | User Outputs DB9 pins 1-4 | [0] = pin1….[3] = pin4 |
| 1403 | Mercury Attenuator (20dB) | [0] = Mercury1….[3] = Mercury4 |
| 1404 | Alex 7 | Reserved for future use |
| 1405 | Alex 7 | Reserved for future use |
| 1406 | Alex 7 | Reserved for future use |
| 1407 | Alex 7 | Reserved for future use |
| 1408 | Alex 6 | Reserved for future use |
| 1409 | Alex6 | Reserved for future use |
| 1410 | Alex6 | Reserved for future use |
| 1411 | Alex 6 | Reserved for future use |
| 1412 | Alex5 | Reserved for future use |
| 1413 | Alex5 | Reserved for future use |
| 1414 | Alex5 | Reserved for future use |
| 1415 | Alex 5 | Reserved for future use |
| 1416 | Alex 4 | Reserved for future use |
| 1417 | Alex 4 | Reserved for future use |
| 1418 | Alex 4 | Reserved for future use |
| 1419 | Alex 4 | Reserved for future use |
| 1420 | Alex 3 | Reserved for future use |
| 1421 | Alex 3 | Reserved for future use |
| 1422 | Alex 3 | Reserved for future use |
| 1423 | Alex 3 | Reserved for future use |
| 1424 | Alex 2 | Reserved for future use |
| 1425 | Alex 2 | Reserved for future use |
| 1426 | Alex 2 | Reserved for future use |
| 1427 | Alex 2 | Reserved for future use |
| 1428 | Alex 1 | Reserved for future use |
| 1429 | Alex 1 | Reserved for future use |
| 1430 | Alex 1 | [15:8] Orion Mk 11 (ANAN-8000DLE) |
| 1431 | Alex 1 | [7:0] Orion Mk 11 (ANAN-8000DLE) |
| 1432 | Alex 0 | [31:24] |
| 1433 | Alex 0 | [23:16] |
| 1434 | Alex 0 | [15:8] |
| 1435 | Alex 0 | [7:0] |
| 1436 | Step Attenuator 7 (0 - 31dB) | Reserved for future use |
| 1437 | Step Attenuator 6 (0 - 31dB) | Reserved for future use |
| 1438 | Step Attenuator 5 (0 - 31dB) | Reserved for future use |
| 1439 | Step Attenuator 4 (0 - 31dB) | Reserved for future use |
| 1440 | Step Attenuator 3 (0 - 31dB) | Reserved for future use |
| 1441 | Step Attenuator 2 (0 - 31dB) | Reserved for future use |
| 1442 | Step Attenuator 1 (0 - 31dB) |  |
| 1443 | Step Attenuator 0 (0 - 31dB) |  |

*Destination Address*

This will be the Ethernet address assigned to the hardware.

*Destination Port*

This may be set using the General packet and if zero defaults to 1027.

*Sequence Number*

A 4-byte integer set to 0x00000000.

*Byte 4*

Bit [0] when set enables the associated SDR hardware and when clear disables. Bit [1] enables transmit of the associated SDR hardware. Bits [2] to [7] are reserved for future use.

*Byte 5*

Bit[0] when set selects CW mode from the Host (e.g. a CW keyboard) with bit[1] and[2] being dot and dash respectively. A set bit will send a dot or dash at the speed selected by the DUC Specific packet.

*Bytes 9 to 12*

These bytes represent a 32bit word that is used to set the frequency of DDC0 in Hz.

*Bytes 13 to 16*

These bytes represent a 32bit word that is used to set the frequency of DDC1 in Hz.

*Bytes 17 to 328*

These bytes represent a 32bit word that is used to set the frequency of DDC2 to DDC79.

*Bytes 329 to 332*

These bytes represent a 32bit word that is used to set the frequency of DUC0 in Hz.

*Byte 345*

This byte sets the power out from DUC0. 0 represents 0 power out and 255 maximum.

*Byte 1400*

This byte is used by the ANAN-8000DLE and decodes as follows:

1. = XVTR\_enable (0 = disabled, 1 = enabled)
2. = IO1 output to enable/mute audio (0=audio enabled, 1= mute)
3. = not assigned
4. = not assigned
5. = not assigned
6. = not assigned
7. = not assigned
8. = not assigned

*Byte 1401*

A set bit enables the associated open collector output. [1] = Open Collector 1, …..[7] = Open Collector 7.

*Byte 1402*

A set bit enables the associated Atlas Metis board User Outputs DB9 connector pins 1-4. [0] = pin1….[3] = pin4

*Byte 1403*

A set bit enables the 20dB attenuate on the associated Atlas Mercury board. [0] = Mercury1….[3] = Mercury4.

*Bytes 1430 to 1435*

These bytes form a 32bit word that selects the various functions on the (Alex) High and Low pass filters, preamplifier and antenna switching. See Appendix D for the mapping of bits to functions.

*Byte 1442*

Selects the attenuation applied to the 0-31dB attenuator before ADC1 (Angelia, Orion, ANAN-100D, ANAN200D only).

*Byte 1443*

Selects the attenuation applied to the 0-31dB attenuator before ADC0 (not Mercury boards).

## DDC AUDIO PACKET

The DDC Audio packet contains left and right audio to be presented to the hardware audio DAC.

It is sent whenever 64 Left and Right audio samples are available. Data defaults to 16 bits per sample at 48ksps.

|  |  |  |
| --- | --- | --- |
|  | **DDC Audio Data (default port 1028)** |  |
| **Byte** | **Data** | **Notes** |
|  |  |  |
| 0 | Seq # | [31:24] |
| 1 | Seq # | [23:16] |
| 2 | Seq # | [15:8] |
| 3 | Seq # | [7:0] |
| 4 | Left Audio Sample 0 | [15:8] |
| 5 | Left Audio Sample 0 | [7:0] |
| 6 | Right Audio Sample 0 | [15:8] |
| 7 | Right Audio Sample 0 | [7:0] |
| 8 | Left Audio Sample 1 | [15:8] |
| 9 | Left Audio Sample 1 | [7:0] |
| 10 | Right Audio Sample 1 | [15:8] |
| 11 | Right Audio Sample 1 | [7:0] |
| …. |  |  |
| …. |  |  |
| 256 | Left Audio Sample 63 | [15:8] |
| 257 | Left Audio Sample 63 | [7:0] |
| 258 | Right Audio Sample 63 | [15:8] |
| 259 | Right Audio Sample 63 | [7:0] |

*Destination Port*

This may be set using the General packet and if zero defaults to 1028.

*Sequence Number*

A 4-byte unsigned integer representing a sequence of packets from this port. The sequence starts at 0x00000000 and rolls over after exceeding 0xFFFFFFFF.

Each port decoder keeps a separate sequence count such that the hardware can determine if a decoder is missing samples in its stream. The sequence number is set to zero at program start or whenever a stop command is sent.

*Bytes 4 to259*

A sequence of 64 2-byte signed integer 2’s Complement values representing demodulated samples for the audio DAC on the hardware. These are sequential in time from the first to last sample.

## DUC I&Q DATA PACKET

The I & Q data packet contains data to be presented to the hardware DUC(n). It is sent whenever 240 I&Q samples are available. Default samples are 24 bits at 192ksps.

|  |  |  |
| --- | --- | --- |
|  | **DUC I&Q Data (default port 1029)** |  |
| **Byte** | **Data** | **Notes** |
|  |  |  |
| 0 | Seq # | [31:24] |
| 1 | Seq # | [23:16] |
| 2 | Seq # | [15:8] |
| 3 | Seq # | [7:0] |
| 4 | I Sample 0 | [23:16] |
| 5 | I Sample 0 | [15:8] |
| 6 | I Sample 0 | [7:0] |
| 7 | Q Sample 0 | [23:16] |
| 8 | Q Sample 0 | [15:8] |
| 9 | Q Sample 0 | [7:0] |
| 10 | I Sample 1 (or Envelope data) | [23:16] |
| 11 | I Sample 1 (or Envelope data) | [15:8] |
| 12 | I Sample 1 (or Envelope data) | [7:0] |
| 13 | Q Sample 1 (or Envelope data) | [23:16] |
| 14 | Q Sample 1 (or Envelope data) | [15:8] |
| 15 | Q Sample 1 (or Envelope data) | [7:0] |
| … |  |  |
| … |  |  |
| 1441 | Q Sample 239 | [23:16] |
| 1442 | Q Sample 239 | [15:8] |
| 1443 | Q Sample 239 | [7:0] |

*Destination Port*

This may be set using the General packet and if zero defaults to 1029 for DAC0. It is automatically incremented by one for each subsequent DAC.

*Sequence Number*

A 4-byte unsigned integer representing a sequence of packets from this port. The sequence starts at 0x00000000 and rolls over after exceeding 0xFFFFFFFF.

Each port decoder keeps a separate sequence count such that the hardware can determine if a decoder is missing samples in its stream. The sequence number is set to zero at program start or whenever a stop command is sent.

*I/Q Sample*

A sequence of 240 3-byte signed integer 2’s Complement I & Q values representing samples for the DUC on the SDR hardware. These are sequential in time from the first to last sample.

NOTE: When Envelope Tracking (ET) or Envelope Elimination & Restoration (EER) mode is selected then alternative I&Q pairs are for DUC and Envelope use respectively.

## MEMORY MAPPED REGISTERS FROM PC

The memory mapped registers from PC packet contains address and data to be sent to the hardware. The format is as follows:

|  |  |  |
| --- | --- | --- |
|  | **Memory Mapped - PC to hardware (default port xxxx)** | |
| **Byte** | **Memory Mapped** | **Notes** |
|  |  |  |
| 0 | Seq # | [31:24] |
| 1 | Seq # | [23:16] |
| 2 | Seq # | [15:8] |
| 3 | Seq # | [7:0] |
| 4 | Address0 | [15:8] |
| 5 | Address0 | [7:0] |
| 6 | Data0 | [31:24] |
| 7 | Data0 | [23:16] |
| 8 | Data0 | [15:8] |
| 9 | Data0 | [7:0] |
| 10 | Address1 | [15:8] |
| 11 | Address1 | [7:0] |
| 12 | Data1 | [31:24] |
| 13 | Data1 | [23:16] |
| 14 | Data1 | [15:8] |
| 15 | Data1 | [7:0] |
| 16 | Address2 | [15:8] |
| 17 | Address2 | [7:0] |
| 18 | Data2 | [31:24] |
| 19 | Data2 | [23:16] |
| 20 | Data2 | [15:8] |
| 21 | Data2 | [7:0] |
| 22 | Address3 | [15:8] |
| 23 | Address3 | [7:0] |
| 24 | Data3 | [31:24] |
| 25 | Data3 | [23:16] |
| 26 | Data3 | [15:8] |
| 27 | Data3 | [7:0] |
| … |  |  |
| 1438 | Address239 | [15:8] |
| 1439 | Address239 | [7:0] |
| 1440 | Data239 | [31:24] |
| 1441 | Data239 | [23:16] |
| 1442 | Data239 | [15:8] |
| 1443 | Data239 | [7:0] |

*Destination Port*

This may be set using the General packet and if zero defaults to xxxx.

*Sequence Number*

A 4-byte unsigned integer representing a sequence of packets from this port. The sequence starts at 0x00000000 and rolls over after exceeding 0xFFFFFFFF.

Each port decoder keeps a separate sequence count such that the hardware can determine if a decoder is missing samples in its stream. The sequence number is set to zero at program start or whenever a stop command is sent.

*Bytes 4 & 5 (en sequence)*

These form the 16 bit address the 32 bit data in the next 4 bytes will be sent to.

*Bytes 6 to 9 (en sequence)*

This form a 32 bit data word that will be sent to the address specified by the address bytes.

## openHPSDR Hardware to Host Protocol

The hardware will communicate with the Host using standard UDP protocol. Byte order shall be MSB first (little Endian) and all values are interpreted as unsigned integers unless otherwise noted. For DFC based software systems Big-Endian or Little-Endian Byte order may be supported in addition to float or double data formats. The Discovery response packet indicates the options available.

IP and UDP headers are as per UDP/IP standards.

Key:

|  |
| --- |
| IP Header (24 bytes) |
| UDP Header (8 bytes) |
| UDP Data (variable bytes) |

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bits  Bytes | 0-7 | 8-15 | 16-23 | 24-31 | 32- 39 | 40-47 | 48-55 | 56-63 |
| 0 | Version/IHL | Type of  Service | Total Length | | Identification | | Flags/Fragment  Offset | |
| 8 | TTL | Protocol | Header Checksum | | Source IP Address | | | |
| 16 | Destination IP Address | | | | IP Options | | | Pad |
| 24 | Source Port | | Destination Port | | UDP Length | | UDP Checksum | |
| 32...  1443 | UDP Data | | | |  | | | |

Future diagrams will only show the UDP Data with a starting byte reference of zero.

## DISCOVERY REPLY PACKET

A Discovery Reply Packet is sent in response to a Host broadcasting a Discovery packet. The Host sends a discovery packet in order to determine what hardware is present on the network and how it is configured.

In order to allow for SDR hardware to provide complete details of all features available two reply formats are provided.

1. Where prior knowledge of the hardware is known by the Host software, and
2. Where the full description of the configuration of the hardware and its capabilities are provided in the response to the Discovery packet.

The data format for option 1 is shown below.

|  |  |  |
| --- | --- | --- |
|  | **Response to Discovery - Hardware to Host (from port 1024)** | |
| **Byte** | **To IP address and Port of Host PC** | **Notes** |
|  |  |  |
| 0 | Seq # = 0 | [31:24] |
| 1 | Seq # = 0 | [23:16] |
| 2 | Seq # = 0 | [15:8] |
| 3 | Seq # = 0 | [7:0] |
| 4 | 0x02 (or 0x03) | Response to Discovery |
| 5 | Board MAC | MSB |
| 6 | Board MAC |  |
| 7 | Board MAC |  |
| 8 | Board MAC |  |
| 9 | Board MAC |  |
| 10 | Board MAC | LSB |
| 11 | Board Type | See Below |
| 12 | openHPSDR Protocol version supported |  |
| 13 | Firmware Code Version |  |
| 14 | Mercury 0 Code Version |  |
| 15 | Mercury 1 Code Version |  |
| 16 | Mercury 2 Code Version |  |
| 17 | Mercury 3 Code Version |  |
| 18 | Penny Code Version |  |
| 19 | Metis Code Version |  |
| 20 | Number of DDCs implemented |  |
| 21 | Frequency or phase word | 0 = frequency 1 = phase |
| 22 | Available Endian modes | See Below |
| 23 | Beta version | 0 = false |
| 24 | Reserved for future use (AD0ES) |  |
| 25 |  |  |
| …. |  |  |
| 59 |  |  |

*Source Port*

This will be set to 1024.

*Destination Port*

This will be set to the Source Port of the Host that initiated the Command.

*Sequence Number*

A 4-byte integer set to 0x00000000.

*Byte 4*

Normally 0x02 but if the hardware is running and already connected to a different Host it will be 0x03.

If byte 4 is 0xFE (0XFF if running) then subsequent bytes contain the hardware configuration of the SDR.

Appendix A describes the format of the hardware configuration.

NOTE: If the reply indicates that the hardware is already connected to a different host then it is recommended that the PC code advise the user that hardware is available but in use. If the user chooses to ignore this message, and proceeds to send appropriate C&C commands, then the hardware will disconnect from the existing connection and connect to the PC sending the C&C commands.

*MAC*

This is 6 bytes and holds the MAC address of the hardware that is responding to the Command request

*Board Type*

A byte interpreted as follows:

|  |
| --- |
| 0: board = "ATLAS" |
| 1: board = “HERMES” (ANAN-10,100) |
| 2: board = “HERMES” (ANAN-10E, 100B) |
| 3: board = “ANGELA” (ANAN-100D) |
| 4: board = “ORION” (ANAN-200D) |
| 5: board = “ORION Mk II” (ANAN-7/8000DLE) |
| 6: board = “Hermes Lite” |
| 7: Reserved |
| 8: Reserved |
| 9: Reserved |
| 10: board = “SATURN” (ANAN-G2) |
| 254: XML hardware description follows |
| 255: Full hardware description follows |

Hardware descriptions for Board types less than 254 are documented in Appendix A. For a Board type of 254 a full hardware description is returned in XML format, see Appendix B. For a Board type of 255 a full hardware description is returned, see Appendix C.

*Byte 12 - Code Version*

A byte that indicates the version of this protocol that the board(s) implement. The Host interprets this as a decimal number e.g. 104 would be interpreted as version 10.4

*Byte 13 - Code Version*

For non-Atlas based systems, a byte that indicates the version of code loaded into the associated board. The Host interprets this as a decimal number e.g. 104 would be interpreted as version 10.4.

*Bytes 14 to 19*

Where an Atlas based system is identified, bytes 13 to 18 contain the code versions loaded into the respective boards. The Host interprets this as a decimal number e.g. 104 would be interpreted as version 10.4. A version number of zero indicates a board is not present.

*Byte 20*

This holds the number of independent DDCs that are implemented in the hardware.

*Byte 21*

This indicates if the hardware requires frequencies to be send as a frequency (Hz) or a phase word. A phase word is calculated as follows:

phase\_word[31:0] = 2^32 \* frequency(Hz)/DSP clock frequency (Hz)

*Byte 22*

This Byte indicates the Endian modes and DDC IQ data formats available as follows:

If Byte 22 is zero then the data format is Big-Endian and I&Q data is in 3 Byte format. If the Byte is not zero then the following options are supported.

Bit 0 = 1 Big-Endian supported

Bit 1 = 1 Little-Endian supported

Bit 2 = 1 3 Byte data format supported

Bit 3 = 1 Float data format supported

Bit 4 = 1 Double data format supported Bits 5, 6 & 7 Reserved for future use.

**NOTE:** The Discovery packet will always use this format irrespective of what Endian mode is selected. The radio can choose from any of these options via the first General packet Byte 39.

*Byte 23 –* If not zero then beta version of code installed.

*Byte 24 –* Reserved

## COMMAND REPLY PACKET

A Command reply packet is returned to the Host making the Command request. The format of the reply is similar to a Discovery reply except that byte 4 (and for Program the sequence number) is different. The reply is returned in response to the following:

*Erase*. Following an EEPROM erase command the hardware will respond with a reply packet that indicates the command has been received and, after the erase is complete – which may take 10’s of seconds, that the erase has been successful. Byte 4 will be set to 0x03.

*Program*. Following a Program command the hardware will respond with a reply packet that indicates that the next 256 bytes of data should be sent by the Host. Byte 4 will be set to 0x04 and the sequence number will be set to the last sequence number received from the Host.

During programming the Host should check the received sequence number in order to verify that a programming packet has been received and in the correct sequence. An incorrect sequence number should be used by the Host to initiate a new Erase and Program cycle. The host should also verify the final checksum matches the checksum of the firmware update file. This will include any filler 0xFF bytes needed to complete the final 256-byte packet. The checksum is the sum of all bytes received and is sent on each program packet reply. The response to a Program command is as follows:

|  |  |  |
| --- | --- | --- |
|  | **Response to Program - Hardware to Host (from port 1024)** | |
| **Byte** | **To IP address and Port of Host PC** | **Notes** |
|  |  |  |
| 0 | Seq # = 0 | [31:24] |
| 1 | Seq # = 0 | [23:16] |
| 2 | Seq # = 0 | [15:8] |
| 3 | Seq # = 0 | [7:0] |
| 4 | 0x04 | Response to Command |
| 5 | Board MAC | MSB |
| 6 | Board MAC |  |
| 7 | Board MAC |  |
| 8 | Board MAC |  |
| 9 | Board MAC |  |
| 10 | Board MAC | LSB |
| 11 | Firmware Code Version |  |
| 12 | Board Type |  |
| 13 | Firmware Checksum | MSB |
| 14 | Firmware Checksum | LSB |
| 15 |  |  |
| … |  |  |
| 59 |  |  |

*Set IP.* Following a successful Set IP command, the hardware will respond with a Discovery reply packet.

## HIGH PRIORITY STATUS PACKET

The High Priority Status packet contains data that indicates the status of the transceiver subsystems. Data representing inputs is sent immediately the data changes, other data is sent periodically. The normal periodic update rate is every 50mS. This is increased to every mS when transmitting in order that the host receives Forward and Reflected Power levels fast enough to display SWR with low latency.

Any change of Status data will be sent as a priority and has precedence over any other packet.

Since actual status changes will be hardware specific the format will vary between different SDR hardware.

The packet format is as follows:

|  |  |  |
| --- | --- | --- |
|  | **Control Elements - Hardware to PC (default port 1025)** | |
| **Byte** | **High Priority** | **Notes** |
|  |  |  |
| 0 | Seq # | [31:24] |
| 1 | Seq # | [23:16] |
| 2 | Seq # | [15:8] |
| 3 | Seq # | [7:0] |
| 4 | Bits - PTT, Dot, Dash | [0] = PTT, [1] = Dot, [2] = Dash, [4] PLL locked, [5]  FIFO almost empty, [6] FIFO almost full |
| 5 | Bits - ADC Overload | [0] = ADC0…[7] = ADC7 |
| 6 | Exciter Power 0 | [15:8] |
| 7 | Exciter Power 0 | [7:0] |
| 8 | Exciter Power 1 | [15:8] Reserved for future use |
| 9 | Exciter Power 1 | [7:0] Reserved for future use |
| 10 | Exciter Power 2 | [15:8] Reserved for future use |
| 11 | Exciter Power 2 | [7:0] Reserved for future use |
| 12 | Exciter Power 3 | [15:8] Reserved for future use |
| 13 | Exciter Power 3 | [7:0] Reserved for future use |
| 14 | Forward Power - Alex 0 | [15:8] (Set to zero if Alex not selected) |
| 15 | Forward Power - Alex 0 | [7:0] (Set to zero if Alex not selected) |
| 16 | Forward Power - Alex 1 | [15:8] Reserved for future use |
| 17 | Forward Power - Alex 1 | [7:0] Reserved for future use |
| 18 | Forward Power - Alex 2 | [15:8] Reserved for future use |
| 19 | Forward Power - Alex 2 | [7:0] Reserved for future use |
| 20 | Forward Power - Alex 3 | [15:8] Reserved for future use |
| 21 | Forward Power - Alex 3 | [7:0] Reserved for future use |
| 22 | Reverse Power - Alex 0 | [15:8] (Set to zero if Alex not selected) |
| 23 | Reverse Power - Alex 0 | [7:0] (Set to zero if Alex not selected) |
| 24 | Reverse Power - Alex 1 | [15:8] Reserved for future use |
| 25 | Reverse Power - Alex 1 | [7:0] Reserved for future use |
| 26 | Reverse Power - Alex 2 | [15:8] Reserved for future use |
| 27 | Reverse Power - Alex 2 | [7:0] Reserved for future use |
| 28 | Reverse Power - Alex 3 | [15:8] Reserved for future use |
| 29 | Reverse Power - Alex 3 | [7:0] Reserved for future use |
| 30 | 0 | Presently unused |
| … |  |  |
| 48 | 0 | Presently unused |
| 49 | Supply Volts | [15:8] |
| 50 | Supply Volts | [7:0] |
| 51 | User ADC3 | [15:8] |
| 52 | User ADC3 | [7:0] |
| 53 | User ADC2 | [15:8] |
| 54 | User ADC2 | [7:0] |
| 55 | User ADC1 | [15:8] |
| 56 | User ADC1 | [7:0] |
| 57 | User ADC0 | [15:8] |
| 58 | User ADC0 | [7:0] |
| 59 | Bits - User logic inputs | [7:0] |

*Source Port*

This may be set using the General packet and if zero defaults to 1025.

*Destination Port*

This will be set to the Source Port of the Host that initiated the Discovery Packet.

*Sequence Number*

A 4-byte integer set to 0x00000000. The sequence starts at 0x00000000 and rolls over after exceeding 0xFFFFFFFF. Each port decoder keeps a separate sequence count such that the Host can determine if a decoder is missing samples in its stream. The sequence number is set to zero at power on or whenever a stop command is received.

*Byte 4*

Bits [0] to [2] indicate the status of an attached PTT button or CW key. A bit is set when the input is active. Bit [4] set indicates that the PLL that locks the master VCXO to the 10MHz internal or external reference is locked. Bit [5] set indicates that the DUC I&Q FIFO is almost empty (<= 511 samples), bit [6] set indicates that the FIFO is almost full (>= 3,840 samples). **NOTE**: DUC I&Q FIFO almost full and almost empty no longer supported.

*Byte 5*

Bits [0] to [7] are set if the associated ADC[n] overload bit is set.

*Bytes 6 & 7*

These form a 16 bit word that represents the forward power from the exciter (or Penelope or Penny Lane boards). The conversion to power is described in Appendix A.

*Bytes 14 & 15*

These form a 16 bit word that represents the forward power from the exciter Power Amplifier. The conversion to power is described in Appendix A.

*Bytes 22 & 23*

These form a 16 bit word that represents the reverse power from the exciter Power Amplifier. The conversion to power is described in Appendix A.

*Bytes 49 & 50*

These form a 16 bit word that represents the supply voltage applied to the hardware (not Atlas bus systems). The conversion to Volts is described in Appendix A.

*Bytes 51 to 58*

These form 16 bit words that represent the general purpose analogue voltage inputs to the hardware. These are presently undefined since they are user specific.

*Byte 59*

Bits [0] to [7] are set if the associated general purpose digital input is set. These are mapped as follows:

1. = IO4 input
2. = IO5 input
3. = IO6 input
4. = IO8 input
5. = IO2 input
6. = not assigned
7. = not assigned
8. = not assigned

## MICROPHONE DATA PACKET

The microphone data packet contains 64 samples from the microphone or line-in inputs on the hardware.

The sample rate is 48ksps and packet format is as follows:

|  |  |  |
| --- | --- | --- |
|  | **Microphone Data (default port 1026)** |  |
| **Byte** | **Data** | **Notes** |
|  |  |  |
| 0 | Seq # | [31:24] |
| 1 | Seq # | [23:16] |
| 2 | Seq # | [15:8] |
| 3 | Seq # | [7:0] |
| 4 | Mic Sample 0 | [15:8] |
| 5 | Mic Sample 0 | [7:0] |
| 6 | Mic Sample 1 | [15:8] |
| 7 | Mic Sample 1 | [7:0] |
| 8 | Mic Sample 2 | [15:8] |
| 9 | Mic Sample 2 | [7:0] |
| 10 | Mic Sample 3 | [15:8] |
| 11 | Mic Sample 3 | [7:0] |
| …. |  |  |
| …. |  |  |
| 128 | Mic Sample 62 | [15:8] |
| 129 | Mic Sample 62 | [7:0] |
| 130 | Mic Sample 63 | [15:8] |
| 131 | Mic Sample 63 | [7:0] |

*Source Port*

This may be set using the General packet and if zero defaults to 1026.

*Destination Port*

This will be set to the Source Port of the Host that initiated the Discovery Packet.

*Sequence Number*

A 4-byte unsigned integer representing a sequence of packets from this port. The sequence starts at 0x00000000 and rolls over after exceeding 0xFFFFFFFF.

Each port decoder keeps a separate sequence count such that the Host can determine if a decoder is missing samples in its stream. The sequence number is set to zero at power on or whenever a stop command is received.

*Mic Sample*

A sequence of 64 2-byte signed integer 2’s Complement values representing samples from the microphone or line-in on the hardware. These are sequential in time from the first to last sample.

## WIDEBAND DATA PACKET

The Wideband data packet contains raw samples from the ADCs selected by the user. The number of bits per sample, number of samples per packet and update rate specified in the General to Hardware settings will be sent when the Wideband enable bit for the associated ADC is set. The Wideband data is intended to be used to display very wide spectral and waterfall displays. Whilst data within a packet, and number of packets set in the General Packet, is time sequential otherwise the data is presented on a block basis so may not be used for real-time demodulation purposes.

The following assumes 512 by 16 bit samples per packet.

|  |  |  |
| --- | --- | --- |
|  | **Wideband Data (default port 1027)** |  |
| **Byte** | **Data** | **Notes** |
|  |  |  |
| 0 | Seq # | [31:24] |
| 1 | Seq # | [23:16] |
| 2 | Seq # | [15:8] |
| 3 | Seq # | [7:0] |
| 4 | Wideband Sample 0 | [15:8] |
| 5 | Wideband Sample 0 | [7:0] |
| 6 | Wideband Sample 1 | [15:8] |
| 7 | Wideband Sample 1 | [7:0] |
| 8 | Wideband Sample 2 | [15:8] |
| 9 | Wideband Sample 2 | [7:0] |
| 10 | Wideband Sample 3 | [15:8] |
| 11 | Wideband Sample 3 | [7:0] |
| …. |  |  |
| …. |  |  |
| 1024 | Wideband Sample 510 | [15:8] |
| 1025 | Wideband Sample 510 | [7:0] |
| 1026 | Wideband Sample 511 | [15:8] |
| 1027 | Wideband Sample 511 | [7:0] |

*Source Port*

This may be set using the General packet and if zero defaults to 1027 for ADC0. The source port is automatically incremented by one for each subsequent Wideband data source.

*Destination Port*

This will be set to the Source Port of the Host that initiated the Discovery Packet.

*Sequence Number*

A 4-byte unsigned integer representing a sequence of packets from this port. The sequence starts at 0x00000000 and rolls over after exceeding 0xFFFFFFFF.

Each port decoder keeps a separate sequence count such that the Host can determine if a decoder is missing samples in its stream. The sequence number is set to zero at power on or whenever a block of raw samples has been sent or whenever a stop command is received.

*ADC Sample*

A sequence of 2-byte signed integer values (default is 512) representing raw samples from the selected ADC on the hardware. These are sequential in time from the first to last sample. Following a request to send wideband data, the sequence number will be set to zero and incremented in each sequential packet until the number of samples set in the General packet has been sent. The sequence number is reset to zero for the next packet or when a stop command is received.

## DDC PACKET

I & Q data from a DDC connected to an ADC will be sent from a UDP port with bits per sample specified by the General settings. I & Q data from either a single DDC or multiple synchronous DDCs can be presented.

The following assumes one DDC using 24 bits per sample.

|  |  |  |
| --- | --- | --- |
|  | **DDC I&Q Data ( DDC0 default port 1035)** |  |
| **Byte** | **Data** | **Notes** |
|  |  |  |
| 0 | Seq # | [31:24] |
| 1 | Seq # | [23:16] |
| 2 | Seq # | [15:8] |
| 3 | Seq # | [7:0] |
| 4 | Time Stamp | [63:56] |
| 5 | Time Stamp | [55:48] |
| 6 | Time Stamp | [47:40] |
| 7 | Time Stamp | [39:32] |
| 8 | Time Stamp | [31:24] |
| 9 | Time Stamp | [23:16] |
| 10 | Time Stamp | [15:8] |
| 11 | Time Stamp | [7:0] |
| 12 | Bits per sample | [15:8] |
| 13 | Bits per sample | [7:0] |
| 14 | I&Q Samples per frame | [15:8] |
| 15 | I&Q Samples per frame | [7:0] |
| 16 | I Sample 0 | [23:16] |
| 17 | I Sample 0 | [15:8] |
| 18 | I Sample 0 | [7:0] |
| 19 | Q Sample 0 | [23:16] |
| 20 | Q Sample 0 | [15:8] |
| 21 | Q Sample 0 | [7:0] |
| 22 | I Sample 1 | [23:16] |
| 23 | I Sample 1 | [15:8] |
| 24 | I Sample 1 | [7:0] |
| 25 | Q Sample 1 | [23:16] |
| 26 | Q Sample 1 | [15:8] |
| 27 | Q Sample 1 | [7:0] |
| … |  |  |
| … |  |  |
| 1441 | Q Sample 237 | [23:16] |
| 1442 | Q Sample 237 | [15:8] |
| 1443 | Q Sample 237 | [7:0] |

*Source Port*

The DDC port will be as allocated by the General Packet and if zero defaults to 1035 for DDC 0.

Each additional DDC will be allocated the next sequential port number e.g. DDC 1 will originate from port 1036.

*Destination Port*

This will be set to the Source Port of the Host that initiated the Discovery Command

*Sequence Number*

A 4-byte unsigned integer representing a sequence of packets from this port. The sequence starts at 0x00000000 and rolls over after exceeding 0xFFFFFFFF.

Each port decoder keeps a separate sequence count such that the Host can determine if a decoder is missing samples in its stream. The sequence number is set to zero at power on or whenever a stop command is received.

*Time stamp*

This is a 64 bit unsigned integer that is incremented at the sample rate of the ADC from which the data is being generated and is set to zero at the 0 to 1 transition of the 1 PPS from a GPS DDC. This complies with the

'Fractional -Seconds Timestamp - The Sample Count Timestamp' of the VITA-49 specification section 6.1.5.1.

*Bits per sample*

A two byte unsigned integer that indicates the number of bits per sample. Current hardware FPGA code supports 24 bits per sample.

*I&Q Samples per frame*

A two byte unsigned integer that indicates the number of samples that follow. The number of samples will not exceed the maximum length of the data payload for a UDP packet and will contain an integer number of I&Q samples. Where synchronous DDC data is presented then the UPD packet will contain an integer number of samples e.g. for two synchronous DDCs [(I0, Q0), (I1, Q1)] x 164.

The data diagram above illustrates the case for one DDC. Should a greater number of synchronous DDCs be used the above data format will be modified accordingly. The number of samples per UDP frame will depend on the width of each I & Q sample i.e. 8, 16, 24, or 32 bits.

*DDC I/Q Samples*

This is a sequence of signed integer 2’s Complement values representing one I or one Q sample from the DDC hardware. These are sequential in time from the first to last sample.

For synchronous DDCs the sample rate of each DDC will be the same and specified by the register settings set using the DDC Specific packet.

NOTE: The sequence of the DDC I&Q samples is represented as ‘I’ samples followed by ‘Q’ samples. There does not appear to be an exact definition as to what constitutes an I or Q sample. In which case when processed by an FFT to resulting spectrum may appear reversed. In which case the I&Q samples should be reversed. However, if samples are considered to be reversed the sequence in which the samples are received will be invariant.

## MEMORY MAPPED REGISTERS FROM HARDWARE

The memory mapped registers from PC packet contains address and data to be sent to the PC. The data should be sent whenever data changes and optionally periodically. The format is as follows:

|  |  |  |
| --- | --- | --- |
|  | **Memory Mapped - Hardware to PC (default port xxxx)** | |
| **Byte** | **Memory Mapped** | **Notes** |
|  |  |  |
| 0 | Seq # | [31:24] |
| 1 | Seq # | [23:16] |
| 2 | Seq # | [15:8] |
| 3 | Seq # | [7:0] |
| 4 | Address0 | [15:8] |
| 5 | Address0 | [7:0] |
| 6 | Data0 | [31:24] |
| 7 | Data0 | [23:16] |
| 8 | Data0 | [15:8] |
| 9 | Data0 | [7:0] |
| 10 | Address1 | [15:8] |
| 11 | Address1 | [7:0] |
| 12 | Data1 | [31:24] |
| 13 | Data1 | [23:16] |
| 14 | Data1 | [15:8] |
| 15 | Data1 | [7:0] |
| 16 | Address2 | [15:8] |
| 17 | Address2 | [7:0] |
| 18 | Data2 | [31:24] |
| 19 | Data2 | [23:16] |
| 20 | Data2 | [15:8] |
| 21 | Data2 | [7:0] |
| 22 | Address3 | [15:8] |
| 23 | Address3 | [7:0] |
| 24 | Data3 | [31:24] |
| 25 | Data3 | [23:16] |
| 26 | Data3 | [15:8] |
| 27 | Data3 | [7:0] |
| … |  |  |
| 1438 | Address239 | [15:8] |
| 1439 | Address239 | [7:0] |
| 1440 | Data239 | [31:24] |
| 1441 | Data239 | [23:16] |
| 1442 | Data239 | [15:8] |
| 1443 | Data239 | [7:0] |

*Destination Port*

This may be set using the General packet and if zero defaults to xxxx.

*Sequence Number*

A 4-byte unsigned integer representing a sequence of packets from this port. The sequence starts at 0x00000000 and rolls over after exceeding 0xFFFFFFFF.

Each port decoder keeps a separate sequence count such that the hardware can determine if a decoder is missing samples in its stream. The sequence number is set to zero at program start or whenever a stop command is sent.

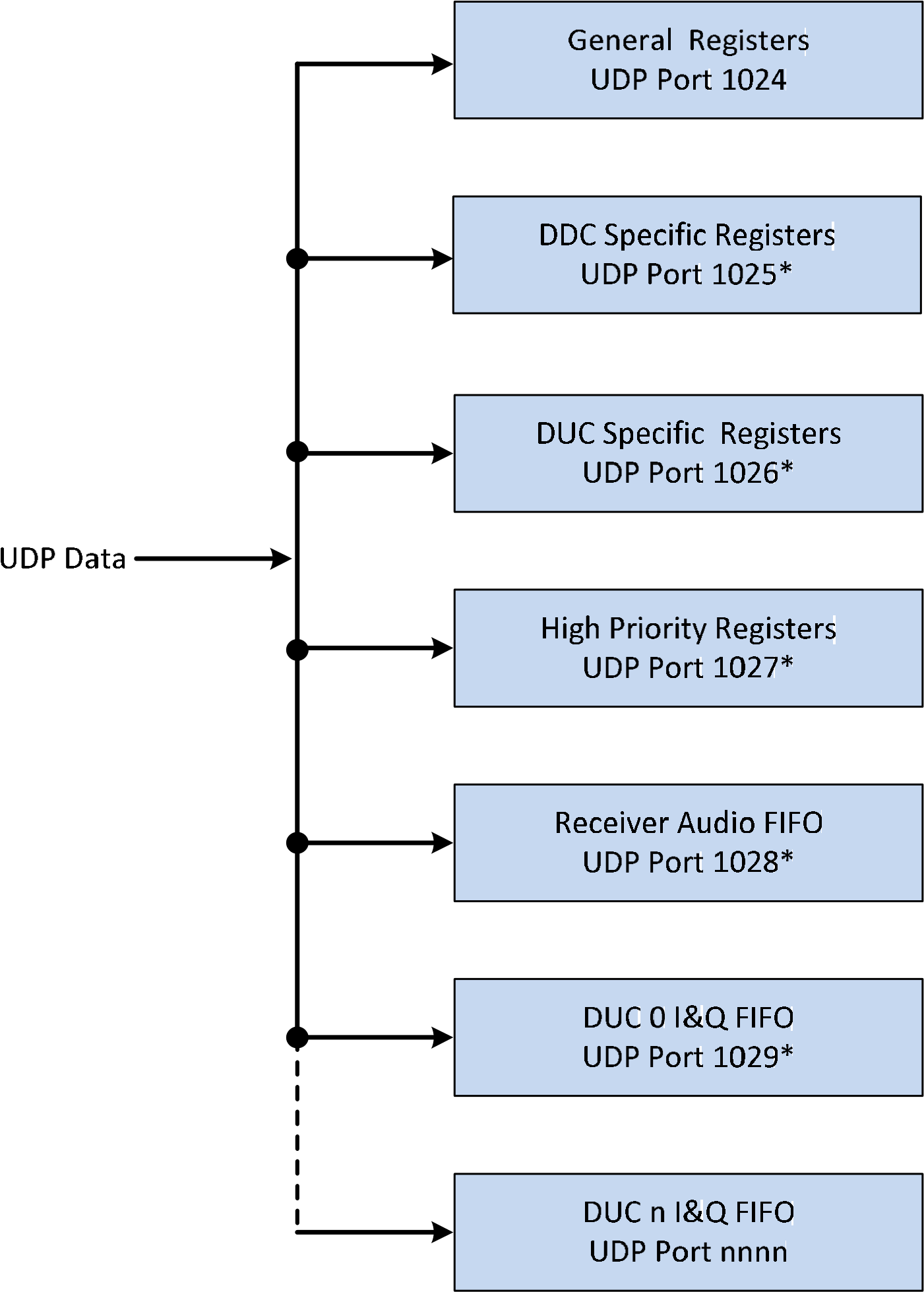
*Bytes 4 & 5 (en sequence)*

These form the 16 bit address the 32 bit data in the next 4 bytes will be sent from.

*Bytes 6 to 9 (en sequence)*

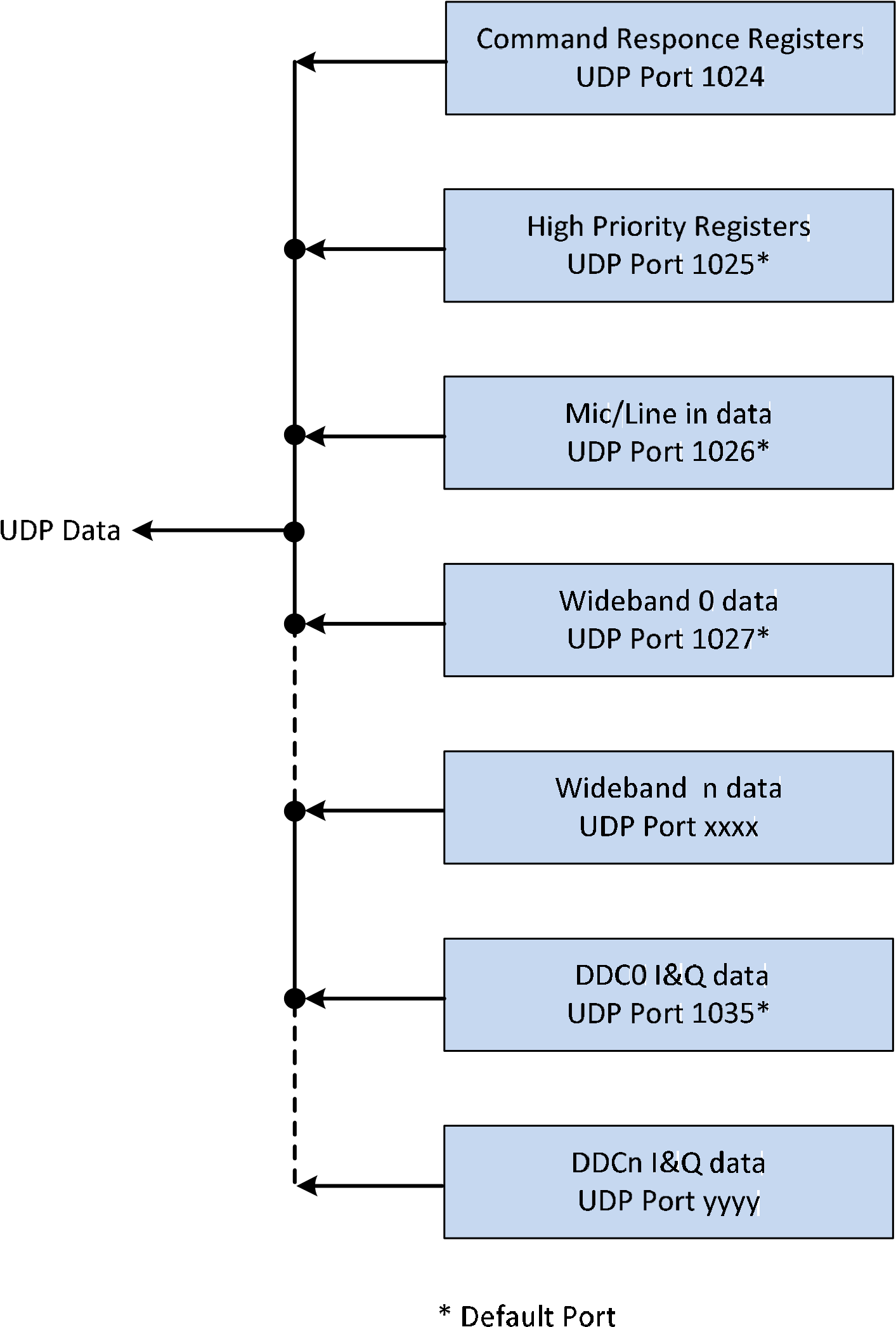
This form a 32 bit data word that is the data contained at the address specified by the address bytes.

## Figure 1 UDP Data from Host





## Figure 2 UDP Data to Host



## Figure 3 DDC Architecture

## Figure 4 DUC Architecture



|  |  |
| --- | --- |
|  | DUC Specific Registers |
|  |

UDP port 1025\*

|  |  |
| --- | --- |
|  | High Priority Registers |
|  |

UDP port 1027\*

\* Default Port

## Appendix A – Hardware capabilities – openHPSDR boards

*Board 0 = Atlas Based Systems*

To be written

*Board 1 = Hermes (ANAN-10, 100)*

|  |  |
| --- | --- |
| **Hardware Capabilities** | |
| Host update of firmware supported | Yes |
| Setting of UDP/IP ports supported | Yes |
| Setting IP address supported | Yes |
| Memory mapped registers supported | No |
| Alex protocol receive filters supported | Yes |
| Alex protocol transmit filters supported | Yes |
| VITA-49 protocol supported | No |
| DSP clock frequency (Hz) | 122.88MHz |
| Number of RF ADCs | 1 |
| Dither supported | Yes |
| Random supported | Yes |
| Number of DDCs supported | TBA |
| DDC Frequency or Phase Word | Phase |
| Receive attenuator supported | Yes |
| Wideband data supported | Yes |
| Wideband samples per Ethernet packet | 512 |
| Wideband bits per sample fixed or variable | Fixed |
| Wideband bits per sample fixed value | 16 |
| Wideband update rate fixed or variable | Variable |
| Wideband update rate fixed (mS) |  |
| Wideband packets per frame fixed or variable | Variable |
| Wideband packets per frame fixed |  |
| Individual DDC sample rates supported | Yes |
| Minimum DDC sampling rate (ksps) | 48 |
| Maximum DDC sampling rate (ksps) | 1,536 |
| CIC decimation values settable | No |
| Synchronous DDCs supported | Yes (for PureSignal only) |
| DDC Audio CODEC supported | Yes, stereo |
| Audio CODEC sample rate (ksps) | 48 |
| Audio CODEC bits per sample | 16 |
| Audio samples per Ethernet packet | 64 Left, 64 Right |
| Time stamping of I&Q data supported | No |
| Number of DUCs supported | 1 |
| DUC Audio CODEC supported | Yes |
| Microphone supported | Yes |
| Line in supported | Yes |
| Audio CODEC sample rate (ksps) | 48 |
| Audio CODEC bits per sample | 16 |
| Audio samples per Ethernet packet | 64 |
| DUC Frequency or phase word required | Phase |
| DUC I&Q sample rate (ksps) | 192 |
| Bits per I/Q sample | 24 |
| I&Q samples per Ethernet packet (24bits per sample) | 238 I samples, 238 Q samples |
| Envelope Tracking supported | No |
| CW Sidetone supported | Yes |
| CW from the Host supported | Yes |
| CW Iambic Keyer supported | Yes |
| CW break-in supported | Yes |
| Hang supported (mS) | Yes, 1 to 1000 |
| RF Delay supported (mS) | Yes, 1 to 255 |
| DUC Phase shift supported | No |
| Receive attenuator on DUC supported | Yes |
| Open collector outputs supported | 7 |
| DDC Calibration | -138dBm (see Note) |
| Number of General Purpose ADCs | 6 |
| Calibration constant for Supply Voltage. V = ADC value /4095 \* constant | constant = 3.3 |
| Calibration constant for Exciter, FWD & REV power  W = (ADC value/4095 \* constant1)2 / constant2  Sale Exciter to 0 to 1000mW  Scale ANAN-10 FWD & REV 0 to 20W  Scale ANAN-100 FWD & REV 0 – 150W | Constant1 = 3.3  Constant2 = 0.09 (ANAN-10)  Constant2 = 0.095 (ANAN100) |

NOTE: DDC calibration. Calibration level is with a 50 ohm load connected to the antenna input, the DDC set to 20m, 500 Hz bandwidth and is the averaged value of the magnitude of the I&Q samples at the output of the filter i.e. DDC noise floor.

*Board 2 = Hermes (ANAN-10E)*

|  |  |
| --- | --- |
| **Hardware Capabilities** | |
| Host update of firmware supported | No, use Bootloader mode |
| Setting of UDP/IP ports supported | No, use Bootloader mode |
| Setting IP address supported | No, use Bootloader mode |
| Memory mapped registers supported | No |
| Alex protocol receive filters supported | No |
| Alex protocol transmit filters supported | Yes (only used on DUC output) |
| VITA-49 protocol supported | No |
| DSP clock frequency (Hz) | 122,880,000 |
| Number of ADCs | 1 |
| Dither supported | Yes |
| Random supported | Yes |
| Number of DDCs supported | 2 |
| DDC Frequency or Phase Word | Phase |
| Receive attenuator supported | Yes, 0 to 31dB only, no Alex attenuators. |
| Wideband data supported | Yes |
| Wideband samples per Ethernet packet | 512 |
| Wideband bits per sample fixed or variable | Fixed |
| Wideband bits per sample fixed value | 16 |
| Wideband update rate fixed or variable | Fixed |
| Wideband update rate fixed (mS) | 100 |
| Wideband packets per frame fixed or variable | Fixed |
| Wideband packets per frame fixed | 4 |
| Individual DDC sample rates supported | Yes |
| Minimum DDC sampling rate (ksps) | 48 |
| Maximum V sampling rate (ksps) | 1,536 |
| CIC decimation values settable | No |
| Synchronous DDCs supported | Yes (for PureSignal only) |
| DDC Audio CODEC supported | Yes, stereo |
| Audio CODEC sample rate (ksps) | 48 |
| Audio CODEC bits per sample | 16 |
| Audio samples per Ethernet packet | 64 left, 64 Right |
| Time stamping of I&Q data supported | No |
| Number of DUCs supported | 1 |
| DUC Audio CODEC supported | Yes |
| Microphone supported | Yes |
| Line in supported | Yes |
| Audio CODEC sample rate (ksps) | 48 |
| Audio CODEC bits per sample | 16 |
| Audio samples per Ethernet packet | 64 |
| DUC Frequency or phase word required | Phase |
| DUC I&Q sample rate (ksps) | 192 |
| Bits per I/Q sample | 24 |
| DUC I&Q samples per Ethernet packet | 240 I, 240 Q |
| Envelope Tracking supported | No |
| CW Sidetone supported | Yes |
| CW from the Host supported | Yes |
| CW Iambic Keyer supported | Yes |
| CW break-in supported | Yes |
| Hang supported (mS) | Yes, 1 to 1000 |
| RF Delay supported (mS) | Yes, 1 to 255 |
| DUC Phase shift supported | No |
| Receive attenuator on DUC supported | Yes |
| Open collector outputs supported | 7 |
| DDC Calibration | -138dBm (see Note) |
| Number of General Purpose ADCs | 6 |
| Calibration constant for Supply Voltage. V = ADC value /4095 \* constant | constant = 3.3 |
| Calibration constant for Exciter, FWD & REV power  W = (ADC value/4095 \* constant1)2 / constant2  Sale Exciter to 0 to 1000mW  Scale ANAN-10E FWD & REV 0 to 20W | Constant1 = 3.3 Constant2 = 0.09 |

NOTE: DDC calibration. Calibration level is with a 50 ohm load connected to the antenna input, the DDC set to

20m, 500 Hz bandwidth and is the averaged value of the magnitude of the I&Q samples at the output of the filter i.e. DDC noise floor.

*Board 3 = Angelia (ANAN-100D)*

|  |  |
| --- | --- |
| **Hardware Capabilities** | |
| Host update of firmware supported | Yes |
| Setting of UDP/IP ports supported | Yes |
| Setting IP address supported | Yes |
| Memory mapped registers supported | No |
| Alex protocol receive filters supported | Yes |
| Alex protocol transmit filters supported | Yes |
| VITA-49 protocol supported | No |
| DSP clock frequency (Hz) | 122,880,000 |
| Number of ADCs | 2 |
| Dither supported | Yes |
| Random supported | Yes |
| Number of DDCs supported | 7 |
| DDC Frequency or Phase Word | Phase |
| Receive attenuator supported | Yes |
| Wideband data supported | Yes |
| Wideband samples per Ethernet packet | 512 |
| Wideband bits per sample fixed or variable | Fixed |
| Wideband bits per sample fixed value | 16 |
| Wideband update rate fixed or variable | Variable |
| Wideband update rate fixed (mS) |  |
| Wideband packets per frame fixed or variable | Variable |
| Wideband packets per frame fixed |  |
| Individual DDCs sample rates supported | Yes |
| Minimum DDC sampling rate (ksps) | 48 |
| Maximum DDC sampling rate (ksps) | 1,536 |
| DDC I & Q samples per Ethernet packet (24 bits) | 328 I, 328 Q |
| CIC decimation values settable | No |
| Synchronous DDCs supported | Yes |
| DDC Audio CODEC supported | Yes, stereo |
| Audio CODEC sample rate (ksps) | 48 |
| Audio CODEC bits per sample | 16 |
| Audio samples per Ethernet packet | 64 Left, 64 Right |
| Time stamping of I&Q data supported | No |
| Number of DUCs supported | 1 |
| DUC Audio CODEC supported | Yes |
| Microphone supported | Yes |
| Line in supported | Yes |
| Audio CODEC sample rate (ksps) | 48 |
| Audio CODEC bits per sample | 16 |
| Audio samples per Ethernet packet | 64 |
| DUC Frequency or phase word required | Phase |
| DUC I&Q sample rate (ksps) | 192 |
| Bits per I/Q sample | 24 |
| I&Q samples per Ethernet packet (24 bit samples) | 238 I, 238 Q |
| Envelope Tracking supported | No |
| CW Sidetone supported | Yes |
| CW from the Host supported | Yes |
| CW Iambic Keyer supported | Yes |
| CW break-in supported | Yes |
| Hang supported (mS) | Yes, 1 - 1000 |
| RF Delay supported (mS) | Yes, 1 - 255 |
| DUC Phase shift supported | No |
| Receive attenuator on DUC supported | Yes |
| Open collector outputs supported | 7 |
| DDC Calibration | -138dBm (see Note) |
| Number of General Purpose ADCs | 6 |
| Calibration constant for Supply Voltage. V = ADC value /4095 \* constant | constant = 3.3 |
| Calibration constant for Exciter, FWD & REV power  W = (ADC value/4095 \* constant1)2 / constant2  Sale Exciter to 0 to 1000mW  Scale ANAN-100D FWD & REV 0 – 150W | Constant1 = 3.3  Constant2 = 0.095 |

NOTE: DDC calibration. Calibration level is with a 50 ohm load connected to the antenna input, the DDC set to

20m, 500 Hz bandwidth and is the averaged value of the magnitude of the I&Q samples at the output of the filter i.e. DDC noise floor.

*Board 4 = Orion (ANAN-200D)*

|  |  |
| --- | --- |
| **Hardware Capabilities** | |
| Host update of firmware supported | Yes |
| Setting of UDP/IP ports supported | Yes |
| Setting IP address supported | Yes |
| Memory mapped registers supported | No |
| Alex protocol receive filters supported | Yes |
| Alex protocol transmit filters supported | Yes |
| VITA-49 protocol supported | No |
| DSP clock frequency (Hz) | 122,880,000 |
| Number of ADCs | 2 |
| Dither supported | Yes |
| Random supported | Yes |
| Number of DDCs supported | TBA |
| DDC Frequency or Phase Word | Phase |
| DDC attenuator supported | Yes |
| Wideband data supported | Yes |
| Wideband samples per Ethernet packet | 512 |
| Wideband bits per sample fixed or variable | Fixed |
| Wideband bits per sample fixed value | 16 |
| Wideband update rate fixed or variable | Variable |
| Wideband update rate fixed (mS) |  |
| Wideband packets per frame fixed or variable | Variable |
| Wideband packets per frame fixed |  |
| Individual DDC sample rates supported | Yes |
| Minimum DDC sampling rate (ksps) | 48 |
| Maximum DDC sampling rate (ksps) | 1,536 |
| DDC I & Q samples per Ethernet packet (24 bits) | 328 I, 328 Q |
| Synchronous DDCs supported | Yes |
| DDC Audio CODEC supported | Yes, stereo |
| Audio CODEC sample rate (ksps) | 48 |
| Audio CODEC bits per sample | 16 |
| Audio samples per Ethernet packet | 64 left, 64 right |
| Time stamping of I&Q data supported | No |
| Number of DUCs supported | 1 |
| DUC Audio CODEC supported | Yes |
| Microphone supported | Yes |
| Line in supported | Yes |
| Audio CODEC sample rate (ksps) | 48 |
| Audio CODEC bits per sample | 16 |
| Audio samples per Ethernet packet | 64 |
| DUC Frequency or phase word required | Phase |
| DUC I&Q sample rate (ksps) | 192 |
| Bits per I/Q sample | 24 |
| Transmit I&Q samples per Ethernet packet | 240 I, 240 Q |
| Envelope Tracking supported | No |
| CW Sidetone supported | Yes |
| CW from the Host supported | Yes |
| CW Iambic Keyer supported | Yes |
| CW break-in supported | Yes |
| Hang supported (mS) | Yes, 1 - 1000 |
| RF Delay supported (mS) | Yes, 1 - 255 |
| DUC Phase shift supported | No |
| Receive attenuator on DUC supported | Yes |
| Open collector outputs supported | 7 |
| DDC Calibration | -138dBm (See Note) |
| Number of General Purpose ADCs | 6 |
| Calibration constant for Supply Voltage. V = ADC value /4095 \* constant | constant = 5.0 |
| Calibration constant for Exciter, FWD & REV power  W = (ADC value/4095 \* constant1)2 / constant2  Sale Exciter to 0 to 1000mW  Scale ANAN-100 FWD & REV 0 – 150W | Constant1 = 5.0  Constant2 = 0.108 |

NOTE: DDC calibration. Calibration level is with a 50 ohm load connected to the antenna input, the DDC set to

20m, 500 Hz bandwidth and is the averaged value of the magnitude of the I&Q samples at the output of the filter i.e. DDC noise floor.

# APPENDIX B – XML format hardware description

To be written

# APPENDIX C – Hardware capabilities – SPECIFIC

|  |  |  |
| --- | --- | --- |
|  | **Response to Discovery - Hardware to Host (from port 1024)** | |
| **Byte** | **To IP address and Port of Host PC** | **Notes** |
|  |  |  |
| 0 | Seq # = 0 | [31:24] |
| 1 | Seq # = 0 | [23:16] |
| 2 | Seq # = 0 | [15:8] |
| 3 | Seq # = 0 | [7:0] |
| 4 | 0x02 (or 0x03) | Response to Discovery |
| 5 | Board MAC | MSB |
| 6 | Board MAC |  |
| 7 | Board MAC |  |
| 8 | Board MAC |  |
| 9 | Board MAC |  |
| 10 | Board MAC | LSB |
| 11 | Board Type | 255 |
| 12 | openHPSDR Protocol version supported |  |
| 13 | Firmware Code Version |  |
| 14 | Spare |  |
| 15 | Spare |  |
| 16 | Spare |  |
| 17 | Spare |  |
| 18 | Spare |  |
| 19 | Spare |  |
| 20 | Host update of firmware supported |  |
| 21 | Setting of UDP/IP ports supported |  |
| 22 | Setting IP address supported |  |
| 23 | Memory mapped registers supported |  |
| 24 | Alex protocol receive filters supported |  |
| 25 | Alex protocol transmit filters supported |  |
| 26 | VITA-49 protocol supported |  |
| 27 | DSP clock frequency (Hz) | [31:24] |
| 28 | DSP clock frequency (Hz) | [23:16] |
| 29 | DSP clock frequency (Hz) | [15:8] |
| 30 | DSP clock frequency (Hz) | [7:0] |
| 31…35 | Reserved for additional General settings |  |
| 36 | Number of ADCs |  |
| 37 | Dither supported |  |
| 38 | Random supported |  |
| 39 | Number of DDCs supported |  |

|  |  |  |
| --- | --- | --- |
| 40 | Frequency or Phase Word | 0 = frequency 1 = phase |
| 41 | Receive attenuator supported |  |
| 42 | Wideband data supported |  |
| 43 | Wideband samples per Ethernet packet | [15:8] |
| 44 | Wideband samples per Ethernet packet | [7:0] |
| 45 | Wideband bits per sample fixed or variable | 0 = fixed 1 = variable |
| 46 | Wideband bits per sample fixed value |  |
| 47 | Wideband update rate fixed or variable | 0 = fixed 1 = variable |
| 48 | Wideband update rate fixed (mS) |  |
| 49 | Wideband packets per frame fixed or variable | 0 = fixed 1 = variable |
| 50 | Wideband packets per frame fixed |  |
| 51 | Individual DDC sample rates supported |  |
| 52 | Minimum DDC sampling rate (ksps) | [15:8] |
| 53 | Minimum DDC sampling rate (ksps) | [7:0] |
| 54 | Maximum DDC sampling rate (ksps) | [15:8] |
| 55 | Maximum DDCsampling rate (ksps) | [7:0] |
| 56 | CIC decimation values settable |  |
| 57 | Synchronous DDCs supported | 0 = no n = number |
| 58 | (Not currently used) |  |
| 59 | DDC Audio CODEC supported | 0 = no 1 = mono 2 = stereo |
| 60 | Audio CODEC sample rate (ksps) |  |
| 61 | Audio CODEC bits per sample |  |
| 62 | Audio samples per Ethernet packet | [15:8] |
| 63 | Audio samples per Ethernet packet | [7:0] |
| 64 | Time stamping of I&Q data supported |  |
| 65…69 | Reserved for additional DDC settings |  |
| 70 | Number of DUCs supported | 0 = none n = number |
| 71 | DUC Audio CODEC supported |  |
| 72 | Microphone supported |  |
| 73 | Line in supported |  |
| 74 | Audio CODEC sample rate (ksps) |  |
| 75 | Audio CODEC bits per sample |  |
| 76 | Audio samples per Ethernet packet | [15:8] |
| 77 | Audio samples per Ethernet packet | [7:0] |
| 78 | Frequency or phase word required | 0 = frequency 1 = phase |
| 79 | I&Q sample rate (ksps) |  |
| 80 | Bits per I/Q sample |  |
| 81 | I&Q samples per Ethernet packet | [15:8] |
| 82 | I&Q samples per Ethernet packet | [7:0] |
| 83 | Envelope Tracking supported |  |
| 84 | CW Sidetone supported |  |
| 85 | CW from the Host supported |  |
| 86 | CW Iambic Keyer supported |  |
| 87 | CW break-in supported |  |
| 88 | Hang supported (mS) | 0 = no n = max delay [15:8] |
| 89 | Hang supported (mS) | 0 = no n = max delay [7:0] |
| 90 | RF Delay supported (mS) | 0 = no n = max delay |
| 91 | DUC Phase shift supported |  |
| 92 | Receive attenuator on DUC supported |  |
| 93 | Open collector outputs supported | 0 = no n = number |
| 94 | DDC Calibration | [15:8] |
| 95 | DDC Calibration | [7:0] |
| 96 | Number of General Purpose ADCs | [7:0] |
| 97…1439 | For future use |  |

*Source Port*

This will be set to 1024.

*Destination Port*

This will be set to the Source Port of the Host that initiated the Command.

*Sequence Number*

A 4-byte integer set to 0x00000000.

*Byte 4*

Normally 0x02 but if the hardware is running and already connected to a different Host it will be 0x03.

*Bytes 5 to 10 - MAC*

This is 6 bytes and holds the MAC address of the hardware that is responding to the Command request

*Byte 12*

A byte that indicates the openHPSDR Protocol Version supported. The Host interprets this as a decimal number e.g. 104 would be interpreted as version 10.4.

*Byte 13 - Firmware Code Version*

A byte that indicates the version of code loaded into the associated board(s). The Host interprets this as a decimal number e.g. 15 would be interpreted as version 1.5.

*Bytes 14 to 19*

Where an Atlas based system is identified, bytes 14 to 19 contain the code versions loaded into the respective boards. A version number of zero indicates a board is not present.

*Byte 20*

Bit [0] set when openHPSDRProgrammer.exe can be used to update the FPGA code.

*Byte 21*

Bit[0] set when other than default UDP/IP ports can be set.

*Byte 22*

Bit[0] set when openHPSDRProgrammer.exe can be used to set a fixed IP address.

*Byte 23*

Bit[0] set when memory mapped registers supported

*Byte 24*

Bit[0] set when Alex protocol receive filters supported

*Byte 25*

Bit[0] set when Alex protocol transmit filters supported

*Byte 26*

Bit[0] set when VITA-49 protocol supported

*Bytes 27 to 30*

A four byte value representing the DSP clock frequency in Hz

*Byte 36*

A byte indicating the number of ADC available

*Byte 37*

Bit [0] set indicates that ADC dither is supported

*Byte 38*

Bit [0] set indicates that ADC random is supported

*Byte 39*

A byte indicating the number of DDCs supported

*Byte 40*

Bit [0] set when phase words are required, if not set then frequency required.

*Byte 41*

Bit [0] set when DDC input attenuator supported

*Byte 42*

Bit [0] set when wideband (i.e. raw ADC samples) supported

*Bytes 43 and 44*

A 16 bit word indicating the number of wideband samples per Ethernet packet

*Byte 45*

Bit [0] set when variable bits per wideband sample are supported

*Byte 46*

A byte indicating the number of fixed bits per wideband sample

*Byte 47*

Bit [0] set when the wideband update rate is variable

*Byte 48*

A byte indicating the fixed wideband update rate

*Byte 49*

Bit [0] set when the number of wideband packets per frame are variable

*Byte 50*

A byte indicating the fixed number of wideband packets per frame

*Byte 51*

Bit [0] set when individual DDC sample rates are supported

*Bytes 52 and 53*

A 16 bit word indicating the minimum DDC sampling rate

*Bytes 54 and 55*

A 16 bit word indicating the maximum DDC sampling rate

*Byte 56*

Bit [0] set when CIC decimation values settable

*Byte 57*

A byte indicating the number of synchronous DDCs supported, zero equates to none.

*Byte 58*

Not currently used

*Byte 59*

A byte indicating an Audio CODEC is supported, zero equates to no, 1 equates to mono and 2 to stereo

*Byte 60*

A byte indicating the Audio CODECs sampling rate in ksps

*Byte 61*

A byte indicating the Audio CODEC bits per sample

*Byte 62 and 63*

A 16 bit word indicating the number of audio samples per Ethernet packet

*Byte 64*

Bit [0] set when time stamping of I&Q samples is supported

*Byte 70*

A byte indicating the number of DUCs supported, zero equates to none

*Byte 71*

Bit [0] set when a DUC Audio CODEC is supported

*Byte 72*

Bit [0] set when a microphone input to the DUC Audio CODEC is supported

*Byte 73*

Bit [0] set when a line input to the DUC Audio CODEC is supported

*Byte 74*

A byte indicating the Audio CODEC’s sampling rate in ksps

*Byte 75*

A byte indicating the Audio CODEC bits per sample

*Byte 76 and 77*

A 16 bit word indicating the number of audio samples per Ethernet packet

*Byte 78*

Bit [0] set when a DUC phase word is required, if zero then frequency required

*Byte 79*

A byte indicating the transmit I&Q data sample rate in ksps

*Byte 80*

A byte indicating the transmit I&Q data sample size in bits

*Byte 81 and 82*

A 16 bit word indicating the number DUC I&Q samples per Ethernet packet

*Byte 83*

Bit [0] set when an Envelope Tracking or Envelope Elimination and Restoration amplifier is supported

*Byte 84*

Bit [0] set when hardware CW sidetone generation is supported

*Byte 85*

Bit [0] set when CW from host is supported

*Byte 86*

Bit [0] set when an Iambic hardware CW keyer is supported

*Byte 87*

Bit [0] set when CW break-in is supported

*Bytes 89 and 89*

A 16 bit word indicating the maximum delay of CW Hang supported in mS. A zero value indicates not supported

*Byte 90*

A byte indicating the maximum delay of RF Delay supported in mS. A zero value indicates not supported

*Byte 91*

Bit [0] set indicates DUC RF phase shift supported

*Byte 92*

Bit [0] set indicates the DDC front end attenuator may be activated on transmit is supported. A zero value indicates not supported

*Byte 93*

A byte indicating the number of open collector outputs supported. A zero value indicates none.

*Bytes 94 and 95*

A 16 bit word indicating the calibration value for a DDC. The value is the maximum value of an I or Q sample with a RF input of -20dBm at a frequency of 14.200 MHz with the DDC tuned to 14.210 MHz and the sample rate set a 48ksps. This value is intended to enable a bandscope and/or S Meter to be calibrated.

*Byte 96*

A byte indicating the number of general purpose ADCs available. These are typically used to indicate forward and reverse powers, supply voltages and temperatures etc.

# Appendix D – Alex filters description

High Pass Filters (HPF) and Low Pass Filters (LPF) may be used with any openHPSDR board set.

The filters are called ‘Alex’ filters (short for Alexiares) which were initially designed by Graham, KE9H, for use with the original Atlas based hardware. The original Alex filters are currently used with Atlas based hardware, but the design has evolved over time for use with other openHPSDR designs.

The method of controlling the various relays that select filters, 6m pre-amp, antennas and attenuators has not changed significantly over time. In which case this document will refer to Alex filters which implies the Alex data protocol rather than the original Alex hardware.

Whist individual Alex implementations will differ, hence the specific descriptions that follow, the common factor is the use of a 32 bit data word [31:0] that controls the various filters, 6m pre-amp, antenna selection and attenuators.

The top 16 bits [31:16] control LPFs, antenna selection and the antenna change over relay whilst the lower 16 bits [15:0] control HPFs, DDC inputs and attenuators. In general, a set bit activates a relay that selects a filter, antenna or attenuator.

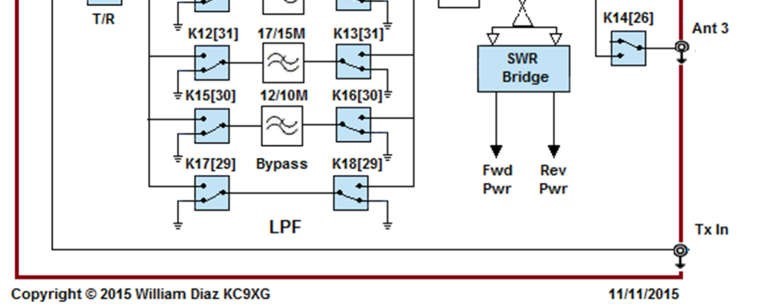
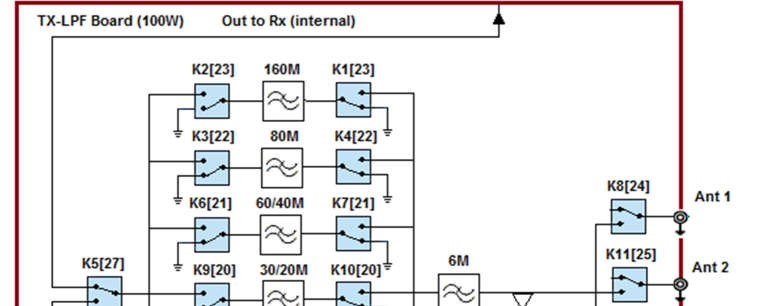
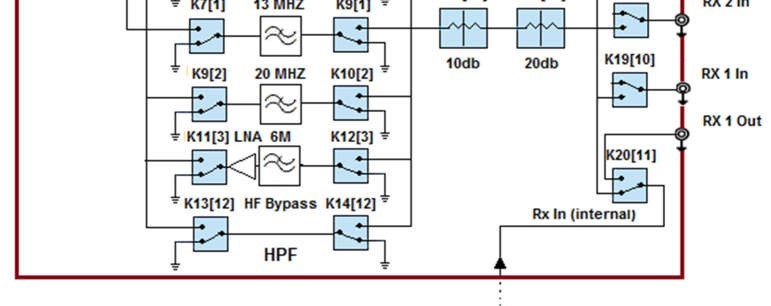
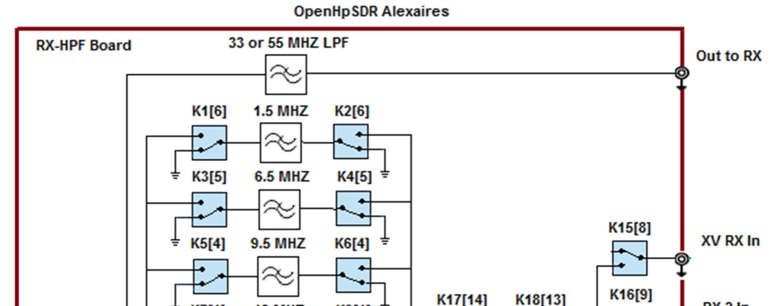
At power on all 32 bits are set to 0 by the FPGA code and remain in that state until an Alex command is received.

In the following block diagrams the numbers against each relay refer to the relay designation in the relevant board schematic followed by the bit that operates it e.g. K2 [23] indicates relay K2 which is operated when bit [23] is set.

Note that in order to use an Alex filter it is necessary to set the relevant bit in Byte 59 of the ‘General to hardware’ packet. Since all existing openHPSDR hardware includes only one Alex filter set, this will mean setting bit [0] of Byte 59.

## ALEX FILTERS FOR ATLAS BASED SYSTEMS

The Alex filters used with Atlas based system comprise two circuit boards, one containing LPFs, Antenna selection and change over relay and the other HPFs, 6m pre-amp, Receive Antenna selection and Attenuators. A block diagram of the filter system is shown in the following diagram.



Relays are shown in de-energised state. The bits in the Alex data register map as follows:

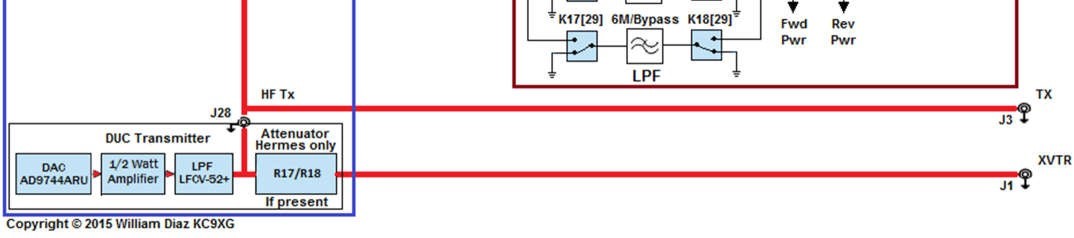
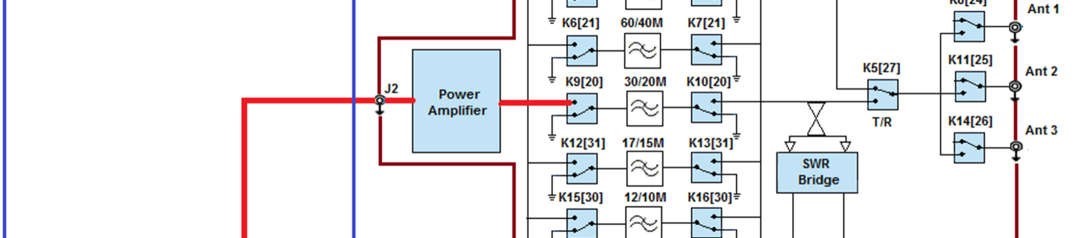
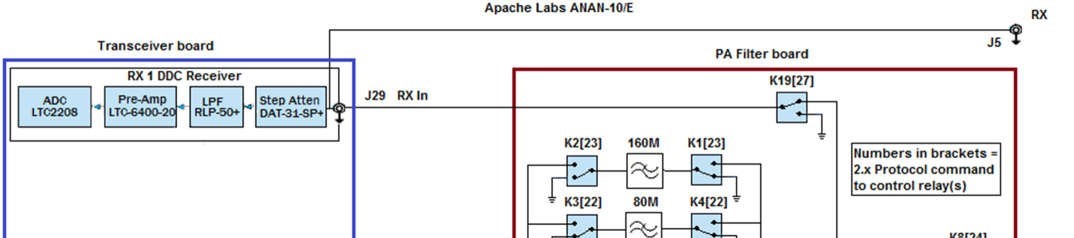
|  |  |  |  |
| --- | --- | --- | --- |
| **Bit** | **Function** | **Bit** | **Function** |
| 0 | YELLOW LED | 16 | N.C. |
| 1 | 13 MHz HPF | 17 | N.C. |
| 2 | 20 MHz HPF | 18 | N.C. |
| 3 | 6M Preamp | 19 | YELLOW LED |
| 4 | 9.5 MHz HPF | 20 | 30/20 Meters LPF |
| 5 | 6.5 MHz HPF | 21 | 60/40 Meters LPF |
| 6 | 1.5 MHz HPF | 22 | 80 Meters LPF |
| 7 | N.C. | 23 | 160 Meters LPF |
| 8 | XVTR DDC In | 24 | ANT 1 |
| 9 | DDC 2 In | 25 | ANT 2 |
| 10 | DDC 1 In | 26 | ANT 3 |
| 11 | DDC 1 Out | 27 | T/R |
| 12 | HF Bypass | 28 | RED LED |
| 13 | 20 dB Atten. | 29 | Bypass |
| 14 | 10 dB Atten. | 30 | 12/10 Meters LPF |
| 15 | RED LED | 31 | 17/15 Meters LPF |

Where all bits are active high and bit 27 high selects transmit.

More details of the board features can be found here: http://openhpsdr.org/alex.php

## ALEX FILTERS FOR ANAN-10 & ANAN-10E SYSTEMS

Both these systems use LPFs only. A block diagram of the filter system is shown in the following diagram.



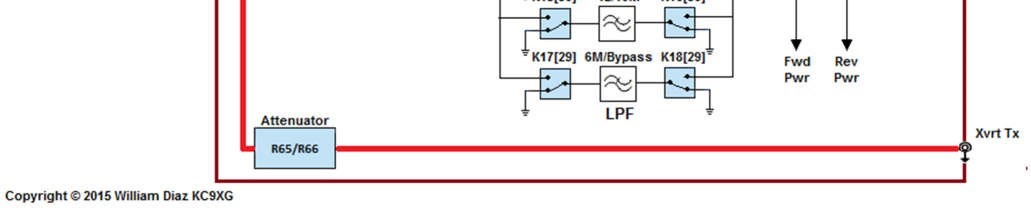
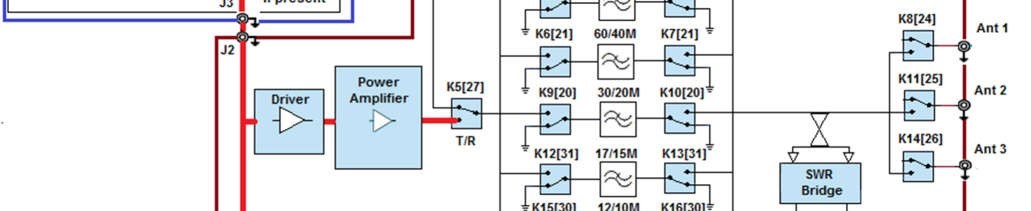
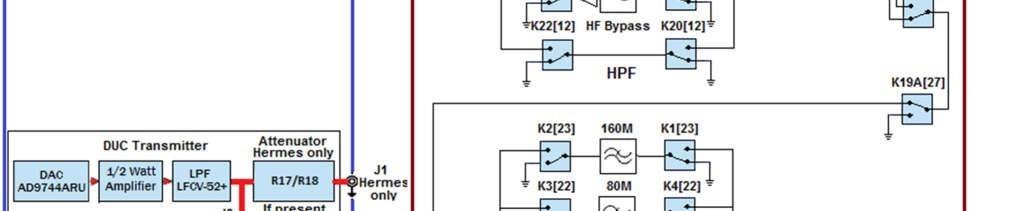
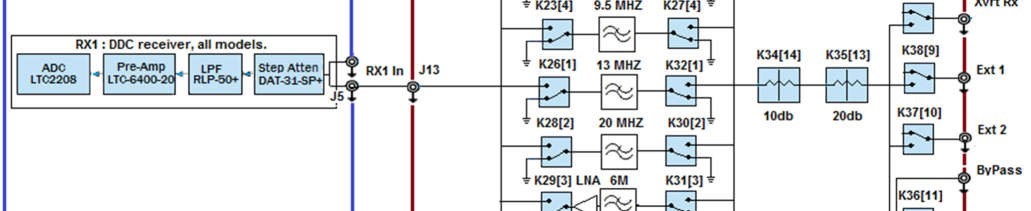
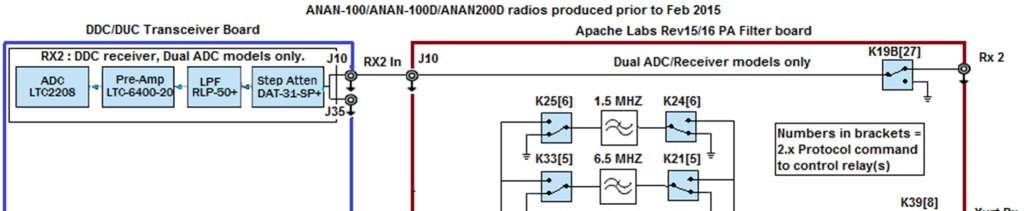
Relays are shown in de-energised state. The bits in the Alex data register map as follows:

|  |  |
| --- | --- |
| **Bit** | **Function** |
| 20 | 30/20 Meters LPF |
| 21 | 60/40 Meters LPF |
| 22 | 80 Meters LPF |
| 23 | 160 Meters LPF |
| 24 | ANT 1 |
| 25 | ANT 2 |
| 26 | ANT 3 |
| 27 | T/R |
| 28 | N.C. |
| 29 | 6 Mtrs/Bypass |
| 30 | 12/10 Meters LPF |
| 31 | 17/15 Meters LPF |

Where all bits are active high and bit 27 high selects transmit.

## ALEX FILTERS FOR ANAN-100, 100D AND 200D SYSTEMS (REV 15/16)

The following block diagram relates to Rev15/16 boards which were fitted prior to **February 2015.**



Relays are shown in de-energised state. The bits in the Alex data register map\* as follows:

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit** | **Function** | **Bit** | **Function** |
| 0 | YELLOW LED | 16 | N.C. |
| 1 | 13 MHz HPF | 17 | N.C. |
| 2 | 20 MHz HPF | 18 | N.C. |
| 3 | 6M Preamp | 19 | YELLOW LED |
| 4 | 9.5 MHz HPF | 20 | 30/20 Meters LPF |
| 5 | 6.5 MHz HPF | 21 | 60/40 Meters LPF |
| 6 | 1.5 MHz HPF | 22 | 80 Meters LPF |
| 7 | N.C. | 23 | 160 Meters LPF |
| 8 | Xvrt DDC | 24 | ANT 1 |
| 9 | Ext 1 | 25 | ANT 2 |
| 10 | Ext 2 | 26 | ANT 3 |
| 11 | ByPass | 27 | T/R |
| 12 | HF Bypass | 28 | RED LED |
| 13 | 20 dB Atten. | 29 | 6M/Bypass |
| 14 | 10 dB Atten. | 30 | 12/10 Meters LPF |
| 15 | RED LED | 31 | 17/15 Meters LPF |

\*For the Orion II (ANAN-8000DLE) the following register map applies:

For Alex 0

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit** | **Function** | **Bit** | **Function** |
| 0 | YELLOW LED | 16 | N.C. |
| 1 | 13 MHz HPF | 17 | N.C. |
| 2 | 20 MHz HPF | 18 | TxRx Status |
| 3 | 6M Preamp | 19 | YELLOW LED |
| 4 | 9.5 MHz HPF | 20 | 30/20 Meters LPF |
| 5 | 6.5 MHz HPF | 21 | 60/40 Meters LPF |
| 6 | 1.5 MHz HPF | 22 | 80 Meters LPF |
| 7 | N.C. | 23 | 160 Meters LPF |
| 8 | N.C. | 24 | ANT 1 |
| 9 | N.C. | 25 | ANT 2 |
| 10 | N.C. | 26 | ANT 3 |
| 11 | N.C. | 27 | T/R |
| 12 | HF Bypass | 28 | RED LED |
| 13 | N.C. | 29 | 6M/Bypass |
| 14 | N.C. | 30 | 12/10 Meters LPF |
| 15 | RED LED | 31 | 17/15 Meters LPF |

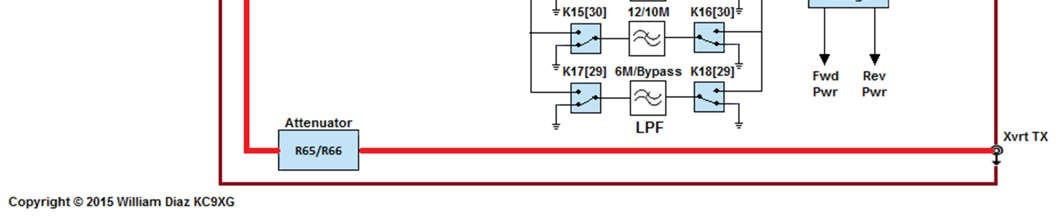
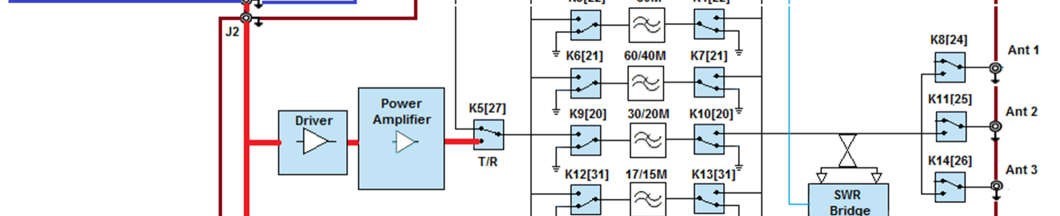
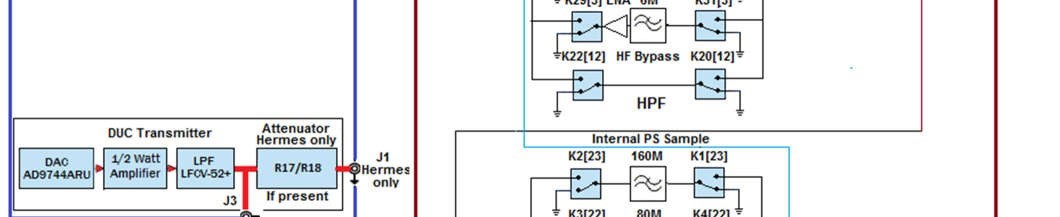
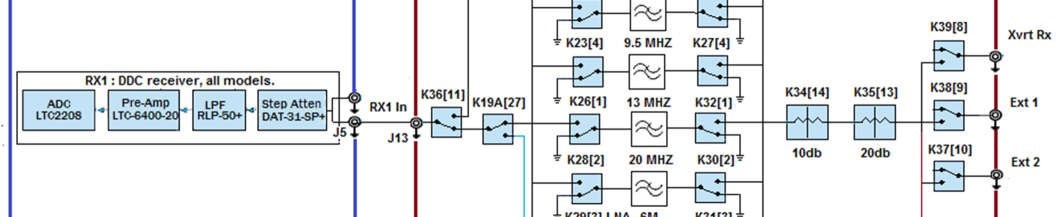
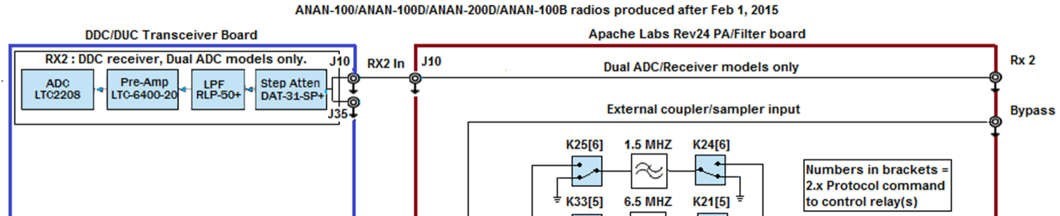
For Alex 1 (HPF)

|  |  |
| --- | --- |
| **Bit** | **Function** |
| 0 | YELLOW LED |
| 1 | 13 MHz HPF |
| 2 | 20 MHz HPF |
| 3 | 6M Preamp |
| 4 | 9.5 MHz HPF |
| 5 | 6.5 MHz HPF |
| 6 | 1.5 MHz HPF |
| 7 | N.C. |
| 8 | Rx2 Ground |
| 9 | N.C. |
| 10 | N.C. |
| 11 | N.C. |
| 12 | HF Bypass |
| 13 | N.C. |
| 14 | N.C. |
| 15 | RED LED |

Where all bits are active high and bit 27 high selects transmit.

## ALEX FILTERS FOR ANAN- 100/100B/100E/200D SYSTEMS (REV 24)

The following block diagram relates to Rev24 boards which were fitted post **February 2015.**

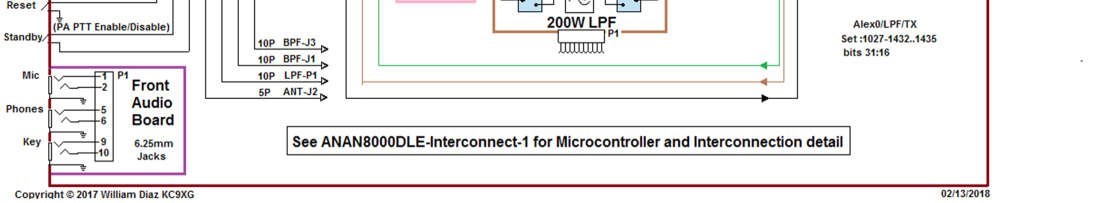
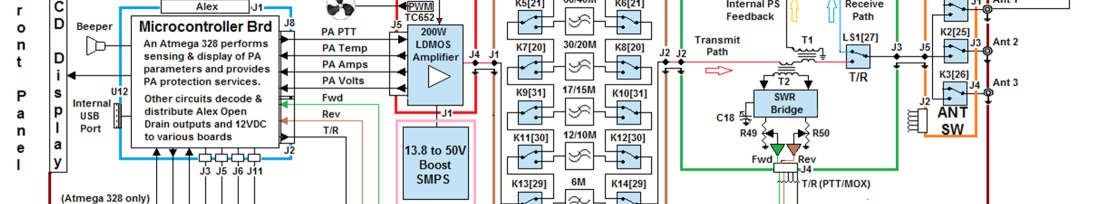
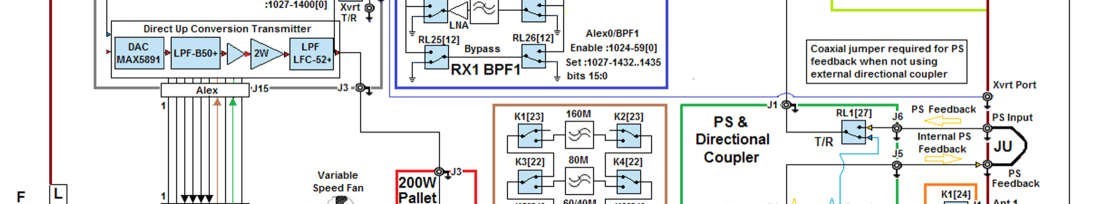
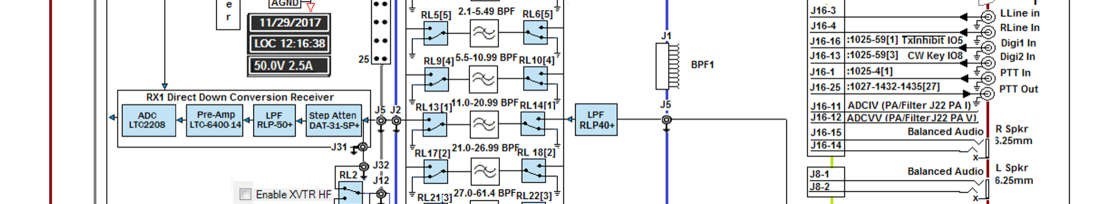
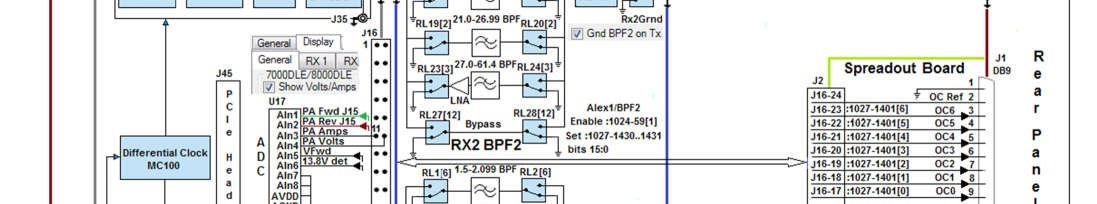
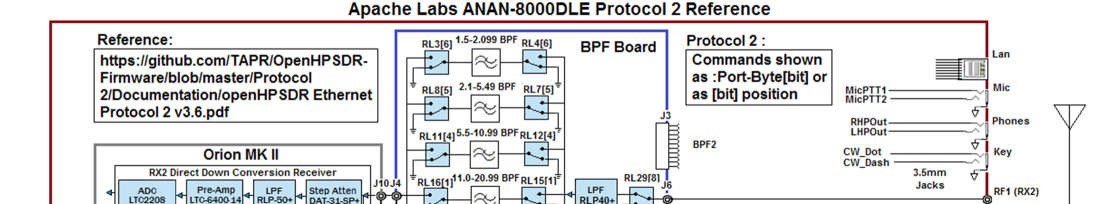


Relays are shown in de-energised state. The bits in the Alex data register (1027-1432..1435) map as follows:

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit** | **Function** | **Bit** | **Function** |
| 0 | YELLOW LED | 16 | N.C. |
| 1 | 13 MHz HPF | 17 | N.C. |
| 2 | 20 MHz HPF | 18 | N.C. |
| 3 | 6M Preamp | 19 | YELLOW LED |
| 4 | 9.5 MHz HPF | 20 | 30/20 Meters LPF |
| 5 | 6.5 MHz HPF | 21 | 60/40 Meters LPF |
| 6 | 1.5 MHz HPF | 22 | 80 Meters LPF |
| 7 | N.C. | 23 | 160 Meters LPF |
| 8 | Xvrt DDC | 24 | ANT 1 |
| 9 | Ext 1 | 25 | ANT 2 |
| 10 | Ext 2 | 26 | ANT 3 |
| 11 | Bypass | 27 | T/R |
| 12 | HF Bypass | 28 | RED LED |
| 13 | 20 dB Atten. | 29 | 6M/Bypass |
| 14 | 10 dB Atten. | 30 | 12/10 Meters LPF |
| 15 | RED LED | 31 | 17/15 Meters LPF |

Where all bits are active high and bit 27 high selects transmit.

## ALEX FILTERS FOR ORION MKII, ANAN-8000DLE



Relays are shown in de-energised state.

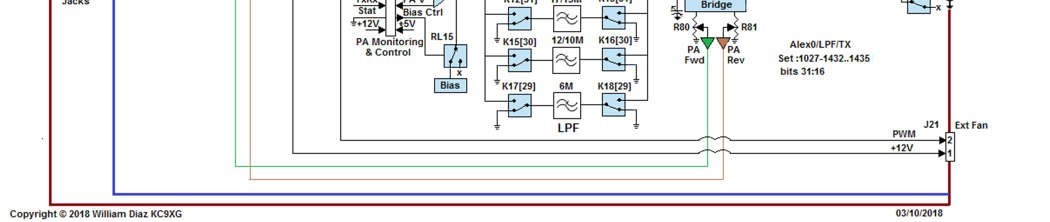
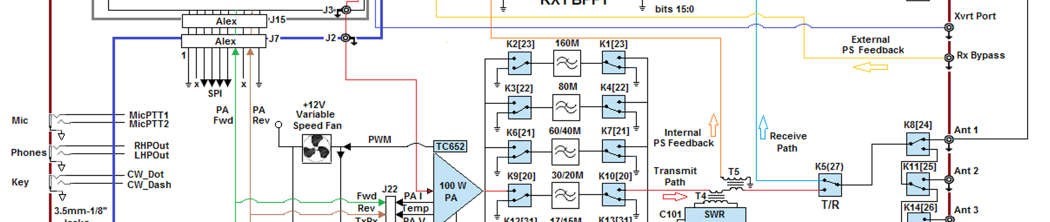
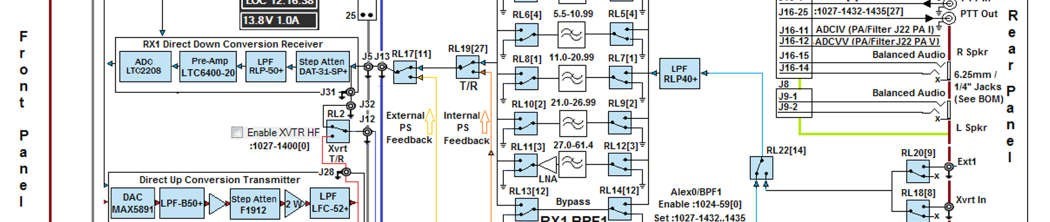
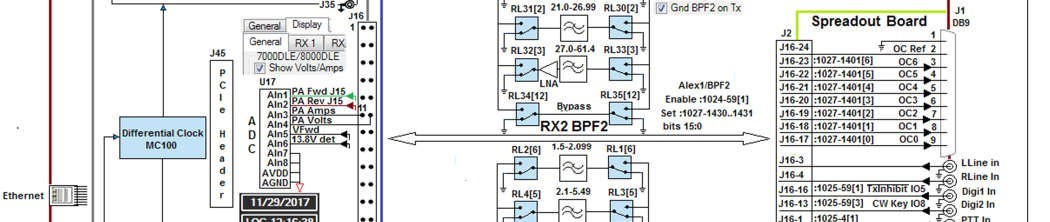
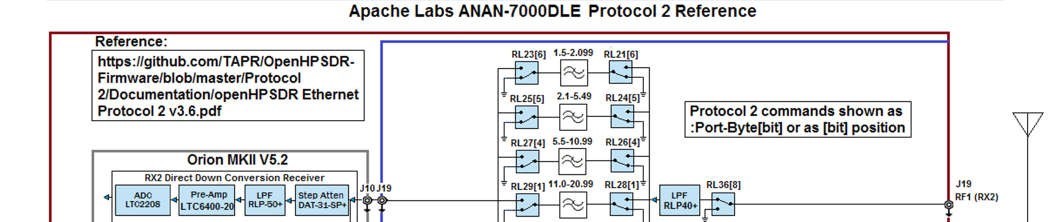
The bits in the Alex 0 data registers (1027-1432..1435) follows:

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit** | **Function** | **Bit** | **Function** |
| 0 | YELLOW LED | 16 | N.C. |
| 1 | 13 MHz BPF | 17 | N.C. |
| 2 | 20 MHz BPF | 18 | TX/RX Status |
| 3 | 6M Preamp | 19 | YELLOW LED |
| 4 | 9.5 MHz BPF | 20 | 30/20 Meters LPF |
| 5 | 6.5 MHz BPF | 21 | 60/40 Meters LPF |
| 6 | 1.5 MHz BPF | 22 | 80 Meters LPF |
| 7 | N.C. | 23 | 160 Meters LPF |
| 8 | N.C. | 24 | ANT 1 |
| 9 | N.C. | 25 | ANT 2 |
| 10 | N.C | 26 | ANT 3 |
| 11 | N.C. | 27 | T/R |
| 12 | HF Bypass | 28 | RED LED |
| 13 | N.C. | 29 | 6M/Bypass |
| 14 | N.C. | 30 | 12/10 Meters LPF |
| 15 | RED LED | 31 | 17/15 Meters LPF |

The bits in the Alex1 (BPF2/RX2) data registers (1027-1430..1431) follow:

|  |  |
| --- | --- |
| Bit | Function |
| 0 | YELLOW LED 2 |
| 1 | 13 MHz BPF 2 |
| 2 | 20 MHz BPF 2 |
| 3 | 6M Preamp 2 |
| 4 | 9.5 MHz BPF 2 |
| 5 | 6.5 MHz BPF 2 |
| 6 | 1.5 MHz BPF 2 |
| 7 | N.C. |
| 8 | RX2 Ground |
| 9 | NC |
| 10 | NC |
| 11 | NC |
| 12 | HPF Bypass 2 |
| 13 | NC |
| 14 | NC |
| 15 | RED LED 2 |

## ALEX FILTERS FOR ORION MKII 5.2, ANAN-7000DLE, SATURN, ANAN-G2



Relays are shown in de-energised state.

The bits in the Alex 0 data registers (1027-1432..1435) follows:

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit** | **Function** | **Bit** | **Function** |
| 0 | YELLOW LED | 16 | N.C. |
| 1 | 13 MHz BPF | 17 | N.C. |
| 2 | 20 MHz BPF | 18 | TX/RX Status |
| 3 | 6M Preamp | 19 | YELLOW LED |
| 4 | 9.5 MHz BPF | 20 | 30/20 Meters LPF |
| 5 | 6.5 MHz BPF | 21 | 60/40 Meters LPF |
| 6 | 1.5 MHz BPF | 22 | 80 Meters LPF |
| 7 | N.C. | 23 | 160 Meters LPF |
| 8 | Xvrt DDC | 24 | ANT 1 |
| 9 | Ext 1 | 25 | ANT 2 |
| 10 | N.C. | 26 | ANT 3 |
| 11 | PS Sample Select | 27 | T/R |
| 12 | HF Bypass | 28 | RED LED |
| 13 | N.C. | 29 | 6M/Bypass |
| 14 | Rx Master in Sel. | 30 | 12/10 Meters LPF |
| 15 | RED LED | 31 | 17/15 Meters LPF |

The bits in the Alex1 (BPF2/RX2) data registers (1027-1430..1431) Follow:

|  |  |
| --- | --- |
| Bit | Function |
| 0 | YELLOW LED 2 |
| 1 | 13 MHz BPF 2 |
| 2 | 20 MHz BPF 2 |
| 3 | 6M Preamp 2 |
| 4 | 9.5 MHz BPF 2 |
| 5 | 6.5 MHz BPF 2 |
| 6 | 1.5 MHz BPF 2 |
| 7 | N.C. |
| 8 | RX2 Ground |
| 9 | N.C. |
| 10 | N.C. |
| 11 | N.C. |
| 12 | HF Bypass 2 |
| 13 | N.C. |
| 14 | N.C. |
| 15 | RED LED 2 |